SSD0300

Advance Information

104 x 48 Dot Matrix
OLED/PLED Segment/Common Driver with Controller

TABLE OF CONTENTS

TABLE OF FIGURES

LIST OF TABLES

1 GENERAL INFORMATION

SSD0300 is a single-chip CMOS OLED/PLED driver with controller for organic/polymer light emitting diode dot-matrix graphic display system. SSD0300 consists of 104 segments, 48 commons that can support a maximum display resolution of 104x48. Besides, there are 4 colours selection to support monochrome or area colour OLED/PLED. This IC is designed for Common Cathode type OLED panel.

SSD0300 embeds with contrast control, display RAM and oscillator, which reduces the number of external components and power consumption. SSD0300 is suitable for many compact portable applications, such as mobile phone sub-display, calculator and MP3 player, etc.

2 FEATURES

- Support maximum 104 x 48 dot matrix panel
- Area colour support with 4 colours selection and 64 steps per colour
- Logic voltage supply: V_{DD}=2.4V - 3.5V
- High voltage supply: V_{CC}=7.0V - 16.0V
- Segment output current: 320uA
- Maximum common sink current: 45mA
- Embedded 104x48 bit SRAM display buffer
- 256-step contrast control on monochrome passive OLED panel
- On-Chip Oscillator
- Programmable Frame Frequency and Multiplexing Ratio
- I^2C interface,8-bit 6800-series Parallel Interface, 8-bit 8080-series Parallel Interface, Serial Peripheral Interface
- Row re-mapping and Column re-mapping
- Vertical scrolling
- Automatic horizontal scrolling function
- Low power consumption
- Wide range of operating temperatures: -40 to 85 °C

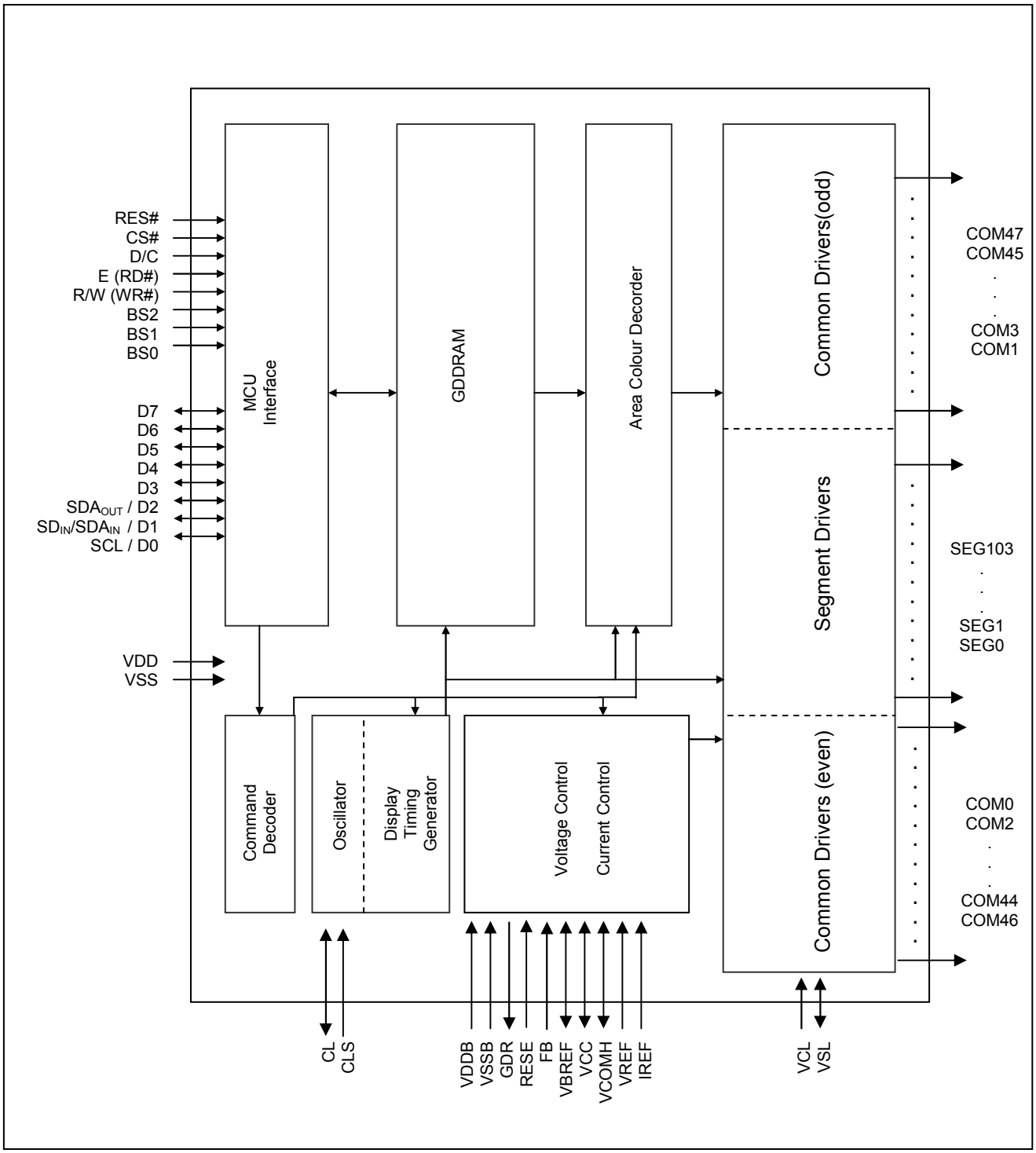
3 ORDERING INFORMATION

Table 1 - Ordering Information

Ordering Part Number	SEG	COM	Package Form	Reference	Remark
SSD0300Z	104	48	Gold Bump Die	Page 6	Die size: 7.29mm x 1.56mm Pad pitch: COM 51.8µm SEG 52.2µm I^2C interface
SSD0300TR1	96	48	TAB	Page 44	• 35mm film • 4 sprocket hole • I^2C interface • Folding TAB • Output lead pitch 0.0997mm
SSD0300T3R1	96	48	TAB	Page 48	• 35mm film • 4 sprocket hole • I^2C interface • Folding TAB • Output lead pitch 0.12974mm

4 BLOCK DIAGRAM

Figure 1 - Block Diagram



5 SSD0300 GOLD-BUMP DIE PAD ASSIGNMENT

Figure 2 - SSD0300Z Pin Assignment

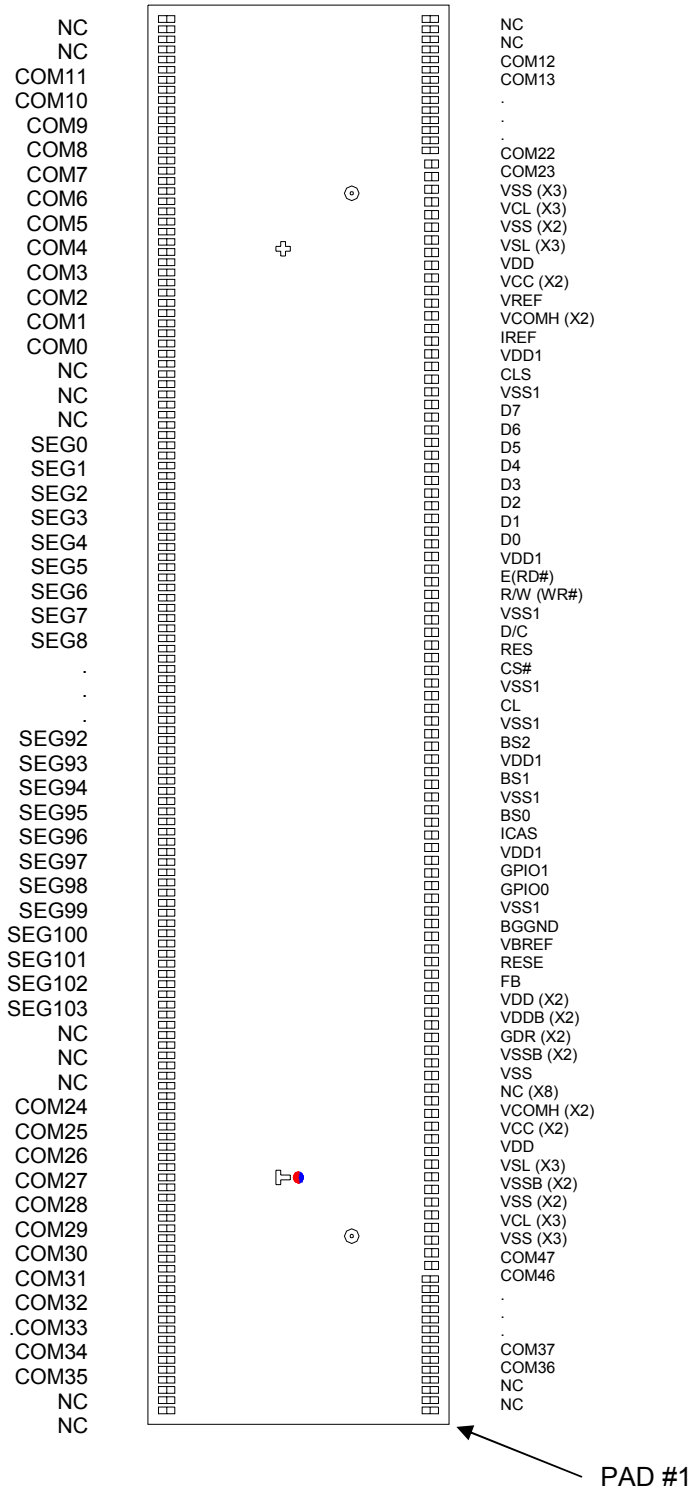
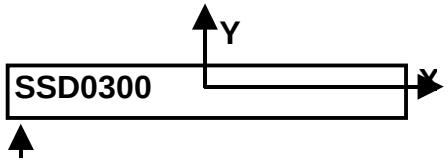


Table 2 - SSD0300Z Die Pad Coordinates

Pad no.	Signal	X-pos	Y-pos
1	NC	-3571.3	-679.6
2	NC	-3519.1	-679.6
3	COM36	-3466.9	-679.6
4	COM37	-3415.1	-679.6
5	COM38	-3363.3	-679.6
6	COM39	-3311.5	-679.6
7	COM40	-3259.7	-679.6
8	COM41	-3207.9	-679.6
9	COM42	-3156.1	-679.6
10	COM43	-3104.3	-679.6
11	COM44	-3052.5	-679.6
12	COM45	-3000.7	-679.6
13	COM46	-2948.9	-679.6
14	COM47	-2897.1	-679.6
15	VSS	-2827.5	-686.6
16	VSS	-2762.5	-686.6
17	VSS	-2697.5	-686.6
18	VCL	-2632.5	-686.6
19	VCL	-2567.5	-686.6
20	VCL	-2502.5	-686.6
21	VSS	-2437.5	-686.6
22	VSS	-2372.5	-686.6
23	VSSBUF	-2307.5	-686.6
24	VSSBUF	-2242.5	-686.6
25	VSL	-2177.5	-686.6
26	VSL	-2112.5	-686.6
27	VSL	-2047.5	-686.6
28	VDD	-1982.5	-686.6
29	VCC	-1917.5	-686.6
30	VCC	-1852.5	-686.6
31	VCOMH	-1787.5	-686.6
32	VCOMH	-1722.5	-686.6
33	NC	-1657.5	-686.6
34	NC	-1592.5	-686.6
35	NC	-1527.5	-686.6
36	NC	-1462.5	-686.6
37	NC	-1397.5	-686.6
38	NC	-1332.5	-686.6
39	NC	-1267.5	-686.6
40	NC	-1202.5	-686.6
41	VSS	-1137.5	-686.6
42	VSSBUF	-1072.5	-686.6
43	VSSBUF	-1007.5	-686.6
44	GDR	-942.5	-686.6
45	GDR	-877.5	-686.6
46	VDDBUF	-812.5	-686.6
47	VDDBUF	-747.5	-686.6
48	VDD	-682.5	-686.6
49	VDD	-617.5	-686.6
50	FB	-552.5	-686.6
51	RESE	-487.5	-686.6
52	VBREF	-422.5	-686.6
53	BGGND	-357.5	-686.6
54	VSS1	-292.5	-686.6
55	GPIO0	-227.5	-686.6
56	GPIO1	-162.5	-686.6
57	VDD1	-97.5	-686.6
58	ICAS	-32.5	-686.6
59	BS0	32.5	-686.6
60	VSS1	97.5	-686.6
61	BS1	162.5	-686.6
62	VDD1	227.5	-686.6
63	BS2	292.5	-686.6
64	VSS1	357.5	-686.6
65	CL	422.5	-686.6
66	VSS1	487.5	-686.6
67	CSB	552.5	-686.6
68	RES	617.5	-686.6
69	D/C	682.5	-686.6
70	VSS1	747.5	-686.6
71	R/W (WR#)	812.5	-686.6
72	E(RD#)	877.5	-686.6
73	VDD1	942.5	-686.6
74	D0	1007.5	-686.6
75	D1	1072.5	-686.6
76	D2	1137.5	-686.6
77	D3	1202.5	-686.6
78	D4	1267.5	-686.6
79	D5	1332.5	-686.6
80	D6	1397.5	-686.6
81	D7	1462.5	-686.6
82	VSS1	1527.5	-686.6
83	CLS	1592.5	-686.6
84	VDD1	1657.5	-686.6
85	IREF	1722.5	-686.6
86	VCOMH	1787.5	-686.6
87	VCOMH	1852.5	-686.6
88	VREF	1917.5	-686.6
89	VCC	1982.5	-686.6
90	VCC	2047.5	-686.6
91	VDD	2112.5	-686.6
92	VSL	2177.5	-686.6
93	VSL	2242.5	-686.6
94	VSL	2307.5	-686.6
95	VSS	2372.5	-686.6
96	VSS	2437.5	-686.6
97	VCL	2502.5	-686.6
98	VCL	2567.5	-686.6
99	VCL	2632.5	-686.6
100	VSS	2697.5	-686.6
101	VSS	2762.5	-686.6
102	VSS	2827.5	-686.6
103	COM23	2897.1	-679.6
104	COM22	2948.9	-679.6
105	COM21	3000.7	-679.6
106	COM20	3052.5	-679.6
107	COM19	3104.3	-679.6
108	COM18	3156.1	-679.6
109	COM17	3207.9	-679.6
110	COM16	3259.7	-679.6
111	COM15	3311.5	-679.6
112	COM14	3363.3	-679.6
113	COM13	3415.1	-679.6
114	COM12	3466.9	-679.6
115	NC	3519.1	-679.6
116	NC	3571.3	-679.6
117	NC	3571.3	679.6
118	NC	3519.1	679.6
119	COM11	3466.9	679.6
120	COM10	3415.1	679.6
121	COM9	3363.3	679.6
122	COM8	3311.5	679.6
123	COM7	3259.7	679.6
124	COM6	3207.9	679.6
125	COM5	3156.1	679.6
126	COM4	3104.3	679.6
127	COM3	3052.5	679.6
128	COM2	3000.7	679.6
129	COM1	2948.9	679.6
130	COM0	2897.1	679.6
131	NC	2844.9	679.6
132	NC	2792.7	679.6
133	NC	2740.5	679.6
134	SEG0	2688.3	679.6
135	SEG1	2636.1	679.6
136	SEG2	2583.9	679.6
137	SEG3	2531.7	679.6
138	SEG4	2479.5	679.6
139	SEG5	2427.3	679.6
140	SEG6	2375.1	679.6
141	SEG7	2322.9	679.6
142	SEG8	2270.7	679.6
143	SEG9	2218.5	679.6
144	SEG10	2166.3	679.6
145	SEG11	2114.1	679.6
146	SEG12	2061.9	679.6
147	SEG13	2009.7	679.6
148	SEG14	1957.5	679.6
149	SEG15	1905.3	679.6
150	SEG16	1853.1	679.6
151	SEG17	1800.9	679.6
152	SEG18	1748.7	679.6
153	SEG19	1696.5	679.6
154	SEG20	1644.3	679.6
155	SEG21	1592.1	679.6
156	SEG22	1539.9	679.6
157	SEG23	1487.7	679.6
158	SEG24	1435.5	679.6
159	SEG25	1383.3	679.6
160	SEG26	1331.1	679.6
161	SEG27	1278.9	679.6
162	SEG28	1226.7	679.6
163	SEG29	1174.5	679.6
164	SEG30	1122.3	679.6
165	SEG31	1070.1	679.6
166	SEG32	1017.9	679.6
167	SEG33	965.7	679.6
168	SEG34	913.5	679.6
169	SEG35	861.3	679.6
170	SEG36	809.1	679.6
171	SEG37	756.9	679.6
172	SEG38	704.7	679.6
173	SEG39	652.5	679.6
174	SEG40	600.3	679.6
175	SEG41	548.1	679.6
176	SEG42	495.9	679.6
177	SEG43	443.7	679.6
178	SEG44	391.5	679.6
179	SEG45	339.3	679.6
180	SEG46	287.1	679.6

Pad no.	Signal	X-pos	Y-pos
181	SEG47	234.9	679.6
182	SEG48	182.7	679.6
183	SEG49	130.5	679.6
184	SEG50	78.3	679.6
185	SEG51	26.1	679.6
186	SEG52	-26.1	679.6
187	SEG53	-78.3	679.6
188	SEG54	-130.5	679.6
189	SEG55	-182.7	679.6
190	SEG56	-234.9	679.6
191	SEG57	-287.1	679.6
192	SEG58	-339.3	679.6
193	SEG59	-391.5	679.6
194	SEG60	-443.7	679.6
195	SEG61	-495.9	679.6
196	SEG62	-548.1	679.6
197	SEG63	-600.3	679.6
198	SEG64	-652.5	679.6
199	SEG65	-704.7	679.6
200	SEG66	-756.9	679.6
201	SEG67	-809.1	679.6
202	SEG68	-861.3	679.6
203	SEG69	-913.5	679.6
204	SEG70	-965.7	679.6
205	SEG71	-1017.9	679.6
206	SEG72	-1070.1	679.6
207	SEG73	-1122.3	679.6
208	SEG74	-1174.5	679.6
209	SEG75	-1226.7	679.6
210	SEG76	-1278.9	679.6
211	SEG77	-1331.1	679.6
212	SEG78	-1383.3	679.6
213	SEG79	-1435.5	679.6
214	SEG80	-1487.7	679.6
215	SEG81	-1539.9	679.6
216	SEG82	-1592.1	679.6
217	SEG83	-1644.3	679.6
218	SEG84	-1696.5	679.6
219	SEG85	-1748.7	679.6
220	SEG86	-1800.9	679.6
221	SEG87	-1853.1	679.6
222	SEG88	-1905.3	679.6
223	SEG89	-1957.5	679.6
224	SEG90	-2009.7	679.6
225	SEG91	-2061.9	679.6
226	SEG92	-2114.1	679.6
227	SEG93	-2166.3	679.6
228	SEG94	-2218.5	679.6
229	SEG95	-2270.7	679.6
230	SEG96	-2322.9	679.6
231	SEG97	-2375.1	679.6
232	SEG98	-2427.3	679.6
233	SEG99	-2479.5	679.6
234	SEG100	-2531.7	679.6
235	SEG101	-2583.9	679.6
236	SEG102	-2636.1	679.6
237	SEG103	-2688.3	679.6
238	NC	-2740.5	679.6
239	NC	-2792.7	679.6
240	NC	-2844.9	679.6

Pad no.	Signal	X-pos	Y-pos
241	COM24	-2897.1	679.6
242	COM25	-2948.9	679.6
243	COM26	-3000.7	679.6
244	COM27	-3052.5	679.6
245	COM28	-3104.3	679.6
246	COM29	-3156.1	679.6
247	COM30	-3207.9	679.6
248	COM31	-3259.7	679.6
249	COM32	-3311.5	679.6
250	COM33	-3363.3	679.6
251	COM34	-3415.1	679.6
252	COM35	-3466.9	679.6
253	NC	-3519.1	679.6
254	NC	-3571.3	679.6



Pad 1,2,3,…->116

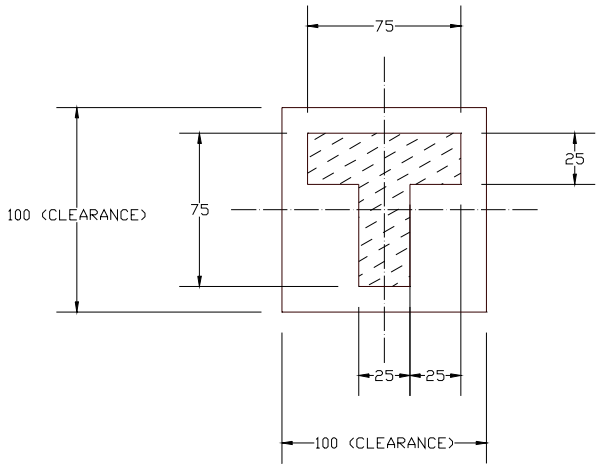
Gold Bumps face up

Die size	7.29mm x 1.56mm
Die height	475 +/- 25um

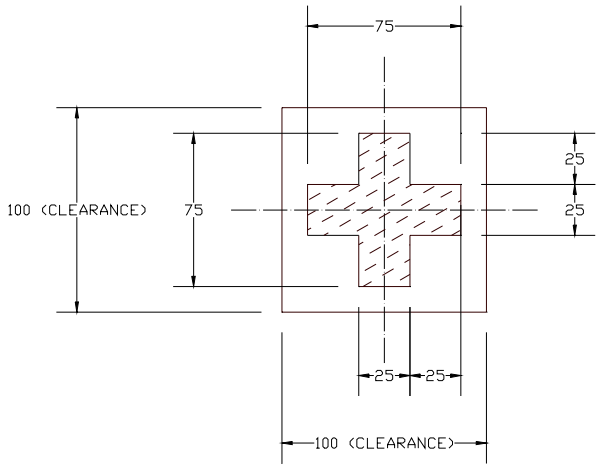
Bump height	Nominal 18um
Bump size	
Pad 1-14, 103-254	34um x 84um
Pad 15-102	42um x 70um

Alignment mark		
T shape	(-2392.0, 79.5)	75um x 75um
+ shape	(2392.0, 79.5)	75um x 76um
Circle	(-2677.0,-274.6)	R37.5um, inner 18um

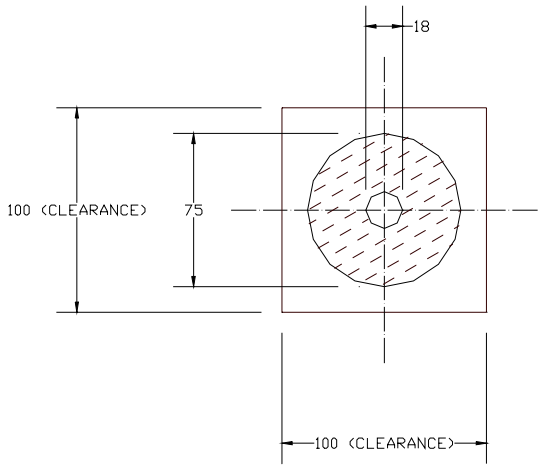
Figure 3 - SSD0300Z Alignment mark dimensions



T shape



+ shape



Circle

Unit in um

6 PIN DESCRIPTION

CL
This pin is the system clock input. When internal clock is enabled, this pin should be left open. The internal clock is output from this pin. When internal oscillator is disabled, this pin receives display clock signal from external clock source.

CLS
This is the internal clock enable pin. When it is pulled HIGH, internal clock is enabled. When it is pulled LOW, the internal clock is disabled; an external clock source must be connected to the CL pin for normal operation.

BS0, BS1, BS2
These are MCU interface input selection pins. See the following table for selecting different interfaces:

	6800-parallel interface	8080-parallel interface	Serial interface	I^2C Interface
BS0	0	0	0	0
BS1	0	1	0	1
BS2	1	1	0	0

CS#
This pin is the chip select input. The chip is enabled for MCU communication only when CS# had been pulled low. Tie to L for I^2C mode application.

RES#
This is a reset signal input pin. When it is pulled LOW, initialization of the chip is executed.

D/C (SA0)
This is the Data/Command control pin. When it is pulled HIGH, the input at D_7-D_0 is treated as display data. When it is pulled LOW, the input at D_7-D_0 is transferred to the command registers. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.
In I^2C mode, this pin act as SA0 for slave address selection

R/W (WR#)
This is a MCU interface input pin. When 6800-series Parallel Interface mode is selected, this pin is used as Read/Write (R/W#) selection input. Pull this pin to HIGH for read mode and pull it to LOW for write mode.
When 8080-series Parallel Interface mode is selected, this pin is used as Write (WR#) selection input. Pull this pin to LOW for write mode. Data write operation is initiated when this pin is pulled LOW and the CS# is pulled LOW.
When I^2C Interface mode is selected, this pin is tied to LOW.

E (RD#)
This is a MCU interface input pin. When 6800-series Parallel Interface is selected, this pin is used as Enable (E) signal. Read/Write operation is initiated when this pin is pulled HIGH and the CS# pin is pulled LOW. When 8080-series Parallel Interface is selected, this pin is used to receive the Read Data (RD#) signal. Data read operation is initiated when this pin is pulled LOW and CS# pin is pulled LOW. When I^2C Interface mode is selected, this pin is tied to LOW.

D_7-D_0
These are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial interface mode is selected, D_1 will be the serial data input, SD_{IN}, and D_0 will be the serial clock input, SCLK.
When I^2C mode is selected, D_2 and D_1 should be tied together and serve as SDA_{OUT}, SDA_{IN} and D_0 is the serial clock input, SCL.

V_{DD}
This is a voltage supply pin. It must be connected to external source.

V_{SS}
This is a ground pin. It also acts as a reference for the logic pins and the OLED driving voltages. It must be connected to external ground.

BGGND
This is a ground pin for analog circuits. It must be connected to external ground

V_{CC}
This is the most positive voltage supply pin of the chip. It should be supplied externally.

V_{REF}
This is a voltage reference pin for pre-charge voltage in driving OLED device. Voltage should be set to match with the OLED driving voltage in current drive phase. It can either be supplied externally or by connecting to VCC.

I_{REF}
This is a segment current reference pin. A resistor should be connected between this pin and V_{SS}. Set the current at 10uA.

V_{COMH}
This is an input pin for the voltage output high level for COM signals. A capacitor should be connected between this pin and VSS.

V_{DDB}
This is a voltage supply pin. It should be connected to V_{DD}.

V_{SSB}
This is a ground pin. It should be connected to V_{SS}.

GDR, RESE, VBREF, FB
These are reserved pins. No connection necessary and should be left open.

COM0-COM47
These pins provide the Common switch signals to the OLED panel. These pins are in high impedance state when display is OFF.

SEG0-SEG103
These pins provide the OLED segment driving signals. These pins are in high impedance stage when display is off.

GPIO0, GPIO1 and ICAS
These are reserved pins. No connection should be made for these pins and left float individually.

VSL
This is a segment voltage reference pin. This pin should be connected to V_{SS} externally.

VCL
This is a common voltage reference pin. This pin should be connected to V_{SS} externally.

V_{DD1}
V_{DD1} is internally connected to V_{DD}. They are for pull high purpose for the neighboring pins if necessary. V_{DD1} can be left open when it is not used.
Main power supply should connect to V_{DD} pins.

V_{SS1}
V_{SS1} is internally connected to V_{SS}. They are for pull low purpose for the neighboring pins if necessary. V_{SS1} can be left open when it is not used.
Main power supply should connect to V_{SS} pin.

NC
These are reserved pins and should not be connected. Do not group or short NC pins.

7 MPU INTERFACES DESCRIPTIONS

MPU I²C Interface

The I²C communication interface consists of slave address bit SA0, I²C-bus data signal SDA (D_2 for output and D_1 for input) and I²C-bus clock signal SCL (D_0). Both the data and clock signals must be connected to pull-up resistors. RES# is used for the initialization of device.

a) Slave address bit (SA0)
SSD0300 has to recognize the slave address before transmitting or receiving any information by the I²C-bus. The device will respond to the slave address following by the slave address bit ("SA0" bit) and the read/write select bit ("R/W#" bit) with the following byte format,
b_7 b_6 b_5 b_4 b_3 b_2 b_1 b_0
0 1 1 1 1 0 SA0 R/W#
"SA0" bit provides an extension bit for the slave address. Either "0111100" or "0111101", can be selected as the slave address of SSD0300.
"R/W#" bit is used to determine the operation mode of the I²C-bus interface. R/W#=1, it is in read mode. R/W#=0, it is in write mode.

b) I²C-bus data signal (SDA)
SDA acts as a communication channel between the transmitter and the receiver. The data and the acknowledgement are sent through the SDA. If SDA in is connected to the "SDA out", the device becomes fully I²C bus compatible.
It should be noticed that the ITO track resistance and the pulled-up resistance at "SDA" pin becomes a voltage potential divider. As a result, the acknowledgement would not be possible to attain a valid logic 0 level in "SDA".
The "SDA out" pin may be disconnected from the "SDA in" pin. With such arrangement, the acknowledgement signal will be ignored in the I²C-bus.

c) I²C-bus clock signal (SCL)
The transmission of information in the I²C-bus is following a clock signal, SCL. Each transmission of data bit is taken place during a single clock period of SCL.

I²C-bus Write data and read register status

The I²C-bus interface gives access to write data and command into the device. Please refer to Figure 4 for the write mode of I²C-bus in chronological order.

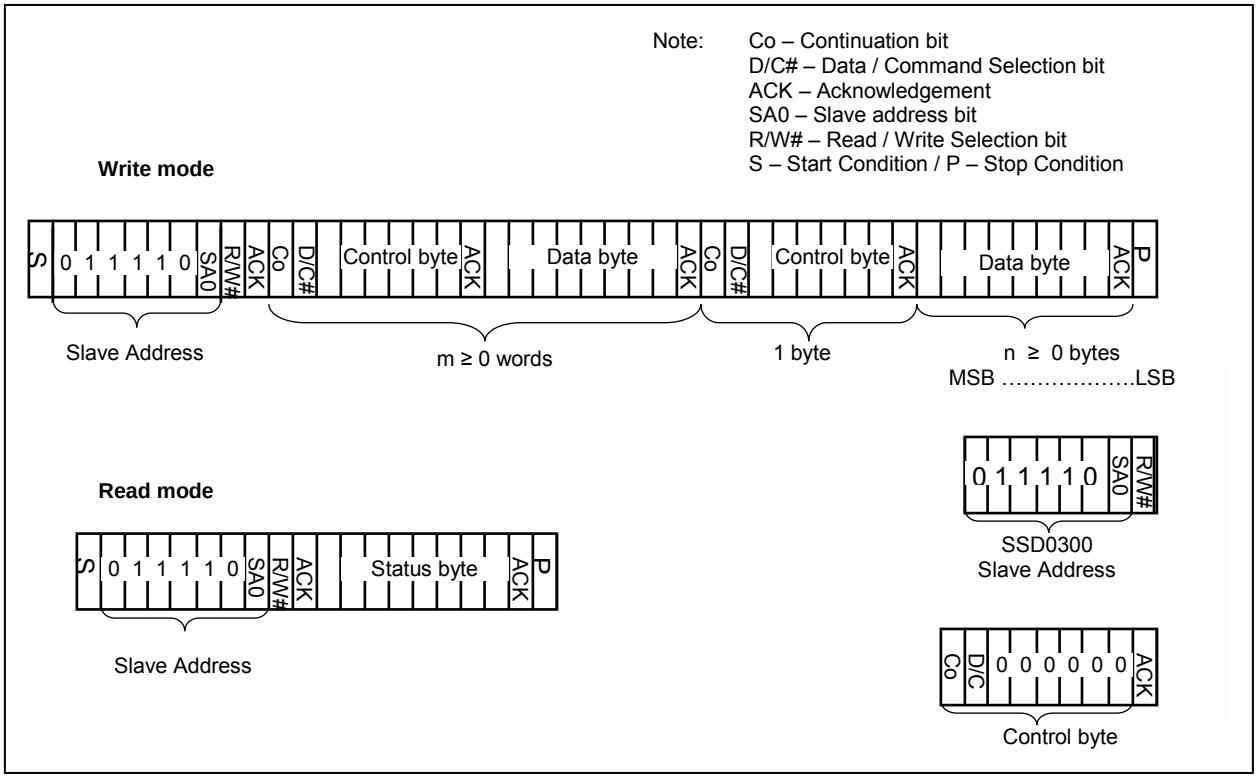


Figure 4 - I²C-bus data format

Write mode for I^2C

1) The master device initiates the data communication by a start condition. The definition of the start condition is shown in Figure 5. The start condition is established by pulling the SDA from HIGH to LOW while the SCL stays HIGH.
2) The slave address is following the start condition for recognition use. For the SSD0300, the slave address is either “b0111100” or “b0111101” by changing the SA0 to HIGH or LOW.
3) The write mode is established by setting the R/W# bit to logic “0”.
4) An acknowledgement signal will be generated after receiving one byte of data, including the slave address and the R/W# bit. Please refer to the Figure 6 for the graphical representation of the acknowledge signal. The acknowledge bit is defined as the SDA line is pulled down during the HIGH period of the acknowledgement related clock pulse.
5) After the transmission of the slave address, either the control byte or the data byte may be sent across the SDA. A control byte mainly consists of Co and D/C# bits following by six “0” ‘s.
    a. If the Co bit is set as logic “0”, the transmission of the following information will contain data bytes only.
    b. The D/C# bit determines the next data byte is acted as a command or a data. If the D/C# bit is set to logic “0”, it defines the following data byte as a command. If the D/C# bit is set to logic “1”, it defines the following data byte as a data which will be stored at the GDDRAM. The GDDRAM column address pointer will be increased by one automatically after each data write.
6) Acknowledge bit will be generated after receiving each control byte or data byte.
7) The write mode will be finished when a stop condition is applied. The stop condition is also defined in Figure 5. The stop condition is established by pulling the “SDA in” from LOW to HIGH while the “SCL” stays HIGH.

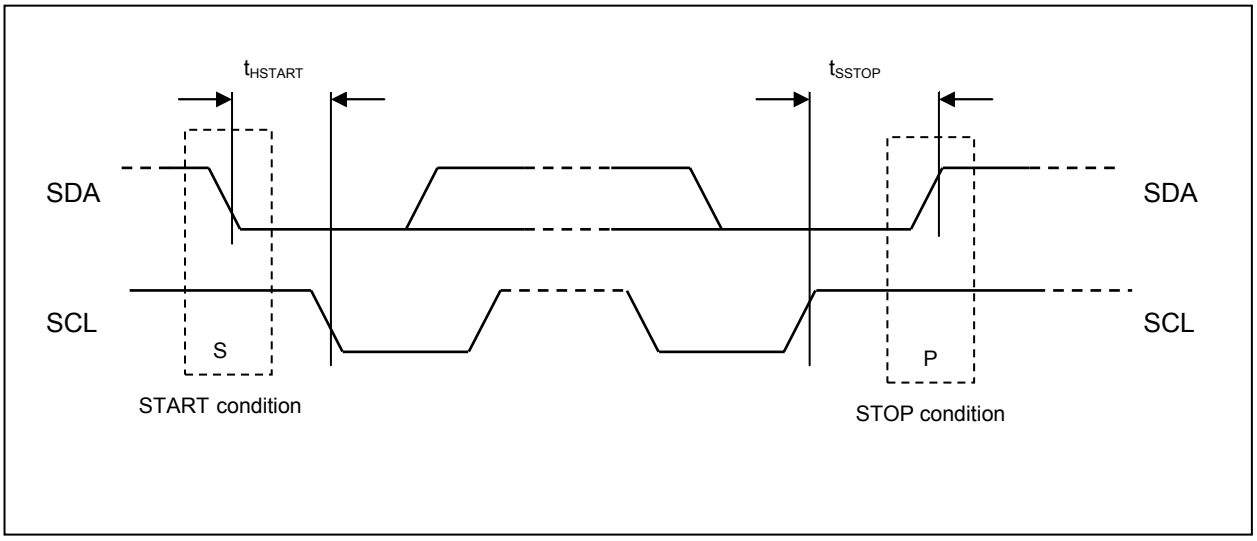


Figure 5 - Definition of the Start and Stop Condition

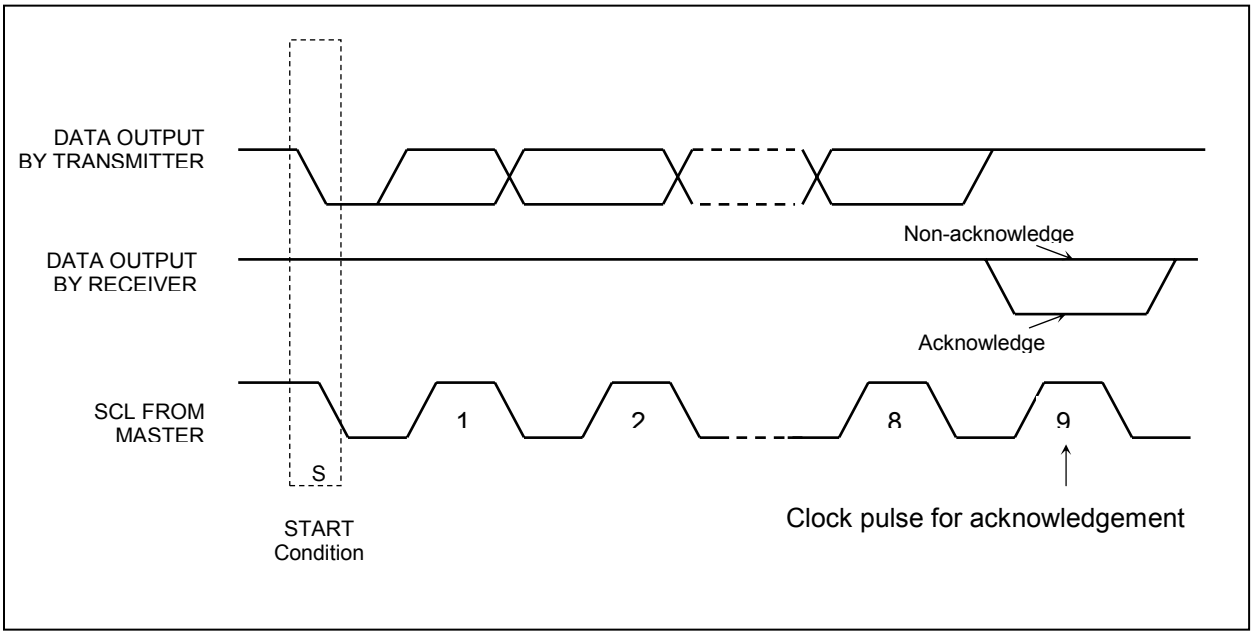


Figure 6 - Definition of the acknowledgement condition

Please be noted that the transmission of the data bit has some limitations.

1. The data bit, which is transmitted during each SCL pulse, must keep at a stable state within the "HIGH" period of the clock pulse. Please refer to the Figure 7 for graphical representations. Except in start or stop conditions, the data line can be switched only when the SCL is LOW.
2. Both the data line (SDA) and the clock line (SCL) should be pulled up by external resistors.

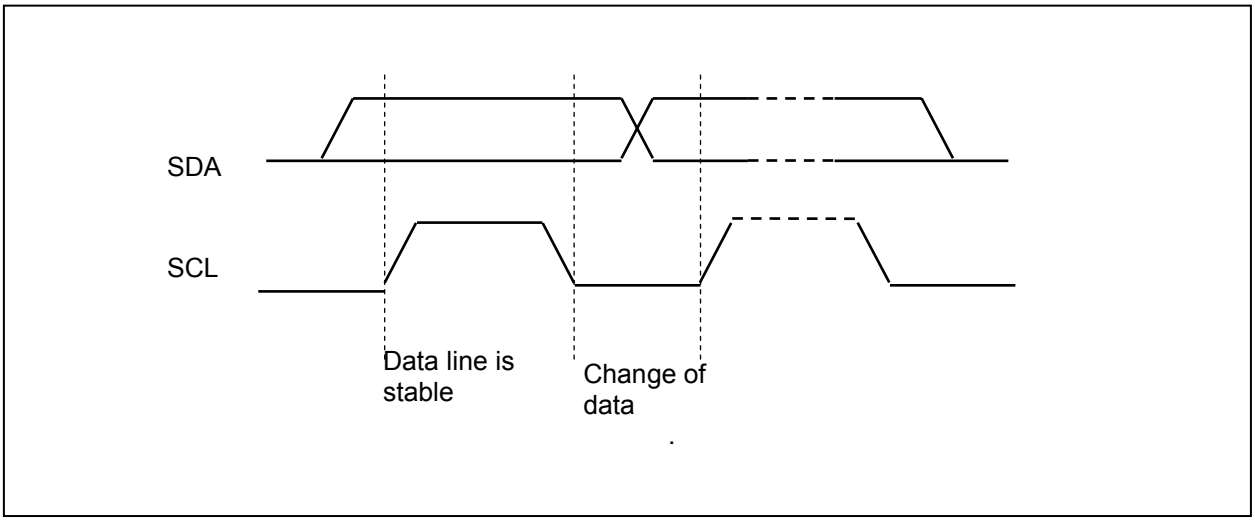


Figure 7 - Definition of the data transfer condition

Read mode for I^2C (Read status register)

1) The master device firstly initiates the data communication by a start condition. The definition of the start condition is shown in Figure 5.
2) The slave address is following the start condition for recognition use. For the SSD0300, the slave address is either “b0111100” or “b0111101”.
3) The read mode is established by setting R/W# bit to logic “1”. The read mode allows the MCU to monitor the internal status of the chip.
4) An acknowledgement signal will be generated after sending one byte of data, including the slave address and the R/W# bit. Please refer to the Figure 6 for the graphical representation of the acknowledge signal.
5) The status of the register will be read at the next status byte. Please refer to the Read Command Table for the explanation of the status byte.
6) The read mode will be finished when a stop condition is applied. The stop condition is also defined in Figure 5.

MPU Parallel 6800-series Interface

The parallel interface consists of 8 bi-directional data pins (D_7-D_0), R/W (WR#), E (RD#), D/C, CS#. When the R/W (WR#) pin is pulled HIGH, Read operation from the Graphic Display Data RAM (GDDRAM) or the status register occurs. When the R/W (WR#) pin is pulled LOW, Write operation to Display Data RAM or Internal Command Registers occurs, depending on the status of D/C input. The E (RD#) input serves as data latch signal (clock) when HIGH provided that CS# is LOW. Refer to Parallel Interface Timing Diagram of 6800-series microprocessors.

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed, which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 8 below.

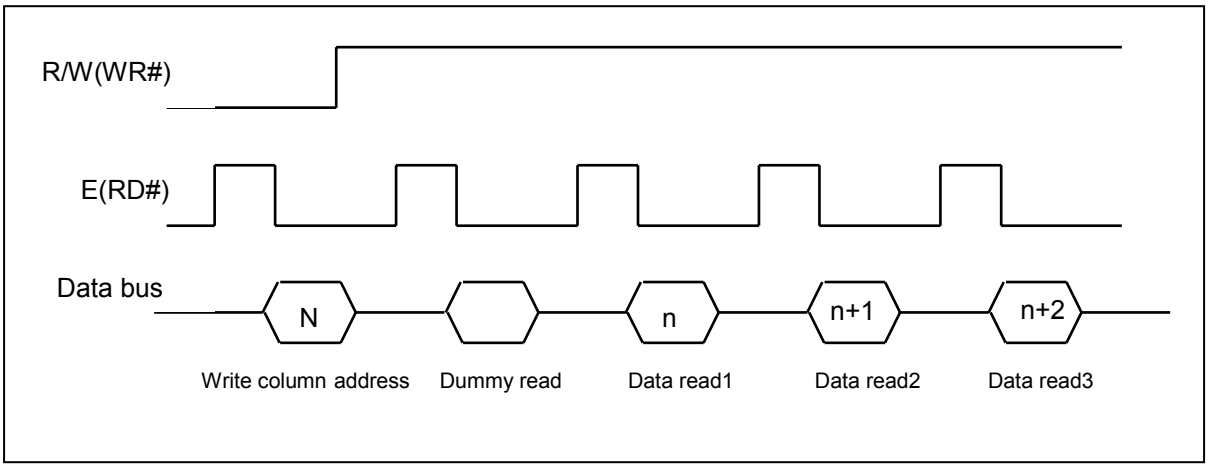


Figure 8 - Display data read back procedure - insertion of dummy read

MPU Parallel 8080-series Interface

The parallel interface consists of 8 bi-directional data pins (D_7-D_0), E (RD#), R/W(WR#), D/C, CS#. The E (RD#) input serves as data read latch signal (clock) when it is low, and provided that CS# is low. Display data or status register read is controlled by D/C.

R/W (WR#) input serves as data write latch signal (clock) when it is high and provided that CS# is low. Display data or command register write is controlled by D/C. Refer to Parallel Interface Timing Diagram of 8080-series microprocessor. Similar to 6800-series interface, a dummy read is also required before the first actual display data read.

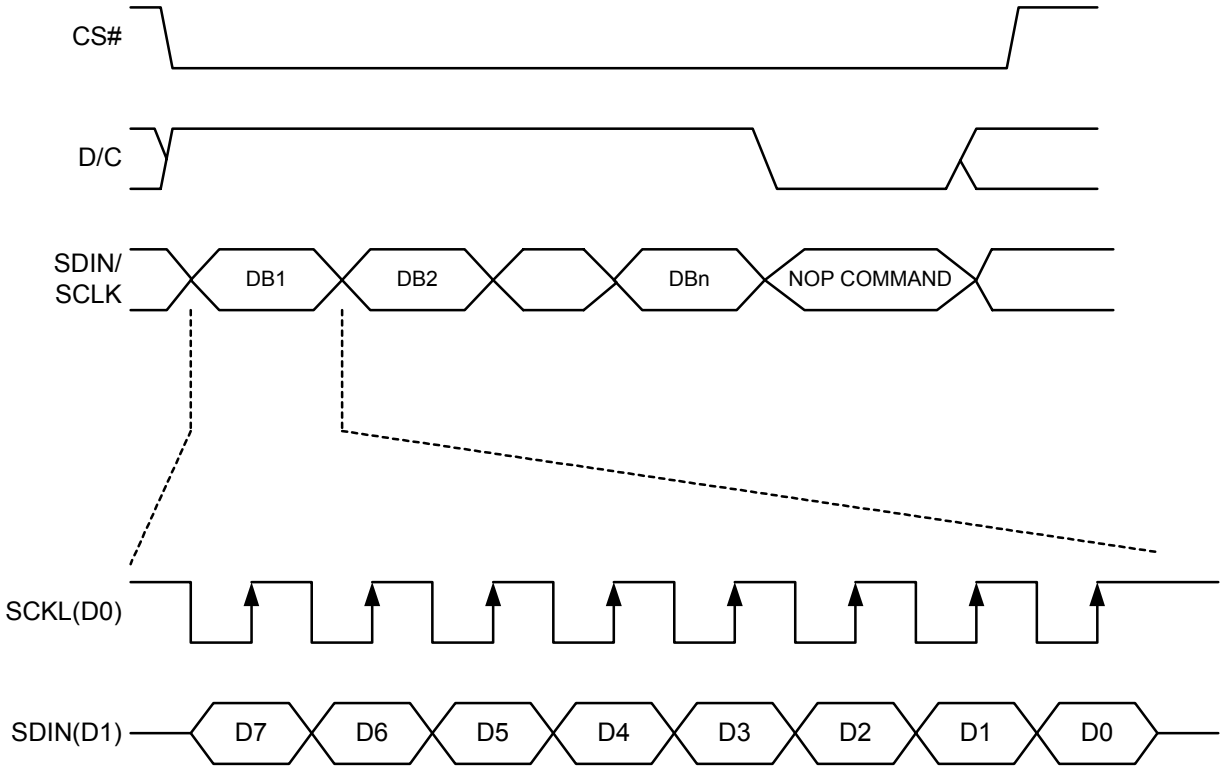
MPU Serial Interface

The serial interface consists of serial clock SCLK, serial data SDIN, D/C, CS#. In SPI mode, D0 acts as SCLK and D1 acts as SDIN. For the unused data pins, D2 should be left open. The pins from D3 to D7, E and R/W can be connected to an external ground.

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D_7, D_6, ... D_0. D/C is sampled on every eighth clock and the data byte in the shift register is written to the Display Data RAM or command register in the same clock.

During data writing, an additional NOP command should be inserted before the CS# goes high (Refer to Figure 9.

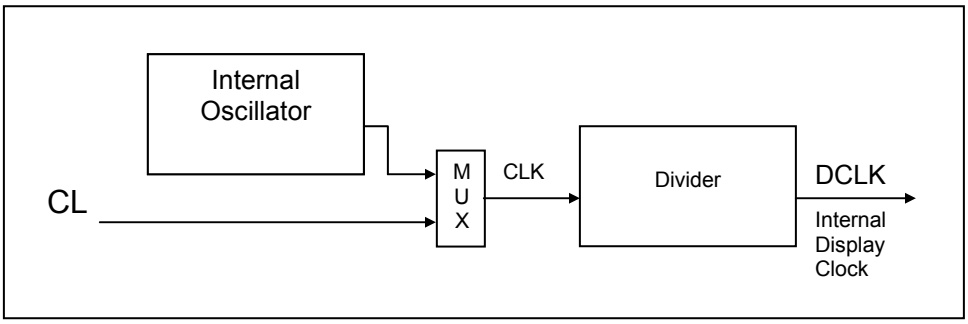
Figure 9 – Display data write procedure in SPI mode



8 FUNCTIONAL BLOCK DESCRIPTIONS

Oscillator Circuit and Display Time Generator

Figure 10 - Oscillator Circuit



This module is an On-Chip low power RC oscillator circuitry (Figure 10). The oscillator generates the clock for the Display Timing Generator.

Reset Circuit

When RES# input is low, the chip is initialized with the following status:

1. Display is OFF
2. 104x48 Display Mode
3. Normal segment and display data column address and row address mapping (SEG0 mapped to column address 00H and COM0 mapped to row address 00H)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 80H
9. Internal DC/DC booster is enable

Command Decoder and Command Interface

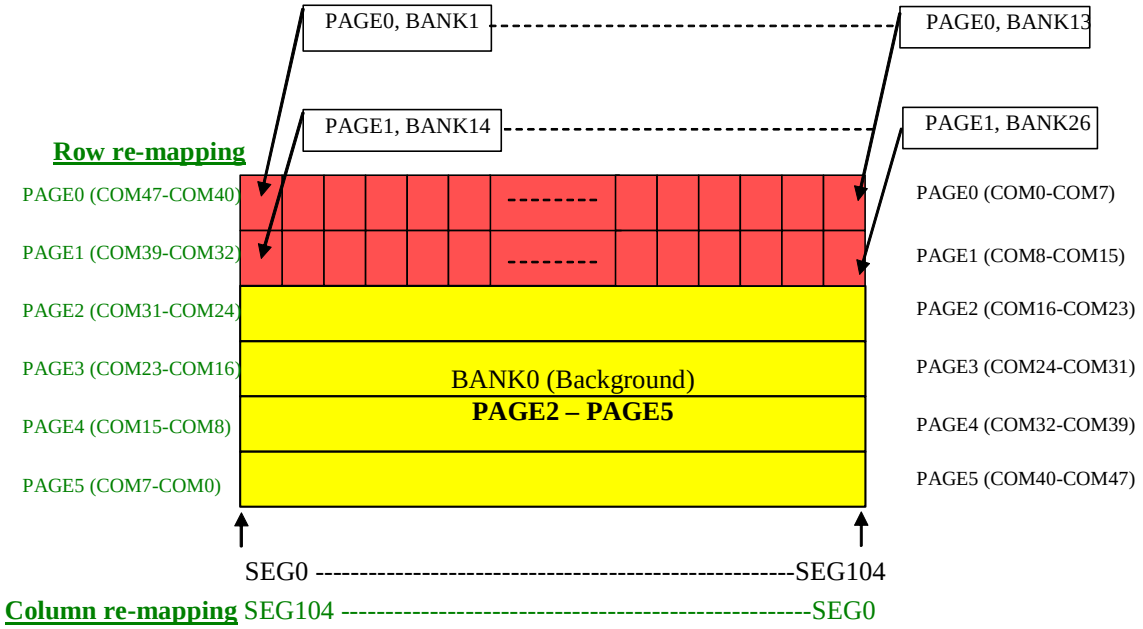
This module determines whether the input data is interpreted as data or command. When the D/C# pin is pulled HIGH, the inputs at D_7-D_0 are interpreted as data and will be written to Graphic Display Data RAM (GDDRAM). When it is pulled LOW, the inputs at D_7-D_0 are interpreted as command, they will be decoded and be written to the corresponding command registers.

Graphic Display Data RAM (GDDRAM)

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 104 x 48 bits and the RAM is divided into six pages, from PAGE0 to PAGE5, as shown in Figure 11. In GDDRAM, PAGE0 and PAGE1 are belonged to area color section with resolution 104x 16. PAGE2 to PAGE5 are used for monochrome 104x 32 dot matrix display.

For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software. For vertical scrolling of the display, an internal register storing display start line can be set to control the portion of the RAM data to be mapped to the display.

Figure 11 - GDDRAM pages structure of SSD0300

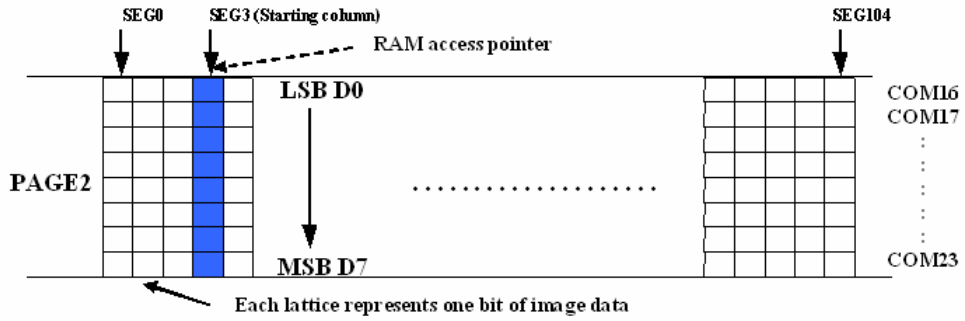


In normal display data RAM read or write mode, the following steps are required to define the starting RAM access pointer location:

- Set the page address of the target display location by command B0h ~ B5h.
- Set the lower column address of pointer by command 00h~0Fh.
- Set the upper column address of pointer by command 10h~1Fh.

For example, if the page address is set to B2h, lower column address is 03h and upper column address is 00h, then that means the starting column is SEG3 of PAGE2. The RAM access pointer is located as shown in Figure 12. The input data byte will be written into RAM position of column 3.

Figure 12 - Example of GDDRAM access location setting (No row re-mapping & column-remapping)



When one data byte is written into GDDRAM, all the rows image data of the same page of the current column are filled (i.e. the whole column (8 bits) pointed by the column address pointer is filled.). Data bit D0 is written into the top row, while data bit D7 is written into bottom row. GDDRAM column address pointer will be increased by one column automatically after each data access. If the current column address pointer points to SEG104, it will point to SEG0 in the same page after the data access. Users have to set the new page address, new lower and upper column address in order to access the next page RAM content.

Current Control and Voltage Control

This block is used to derive the incoming power sources into the different levels of internal use voltage and current. V_{CC} and V_{DD} are external power supplies. V_{REF} is reference voltage, which is used to derive driving voltage for segments and commons. I_{REF} is a reference current source for segment current drivers.

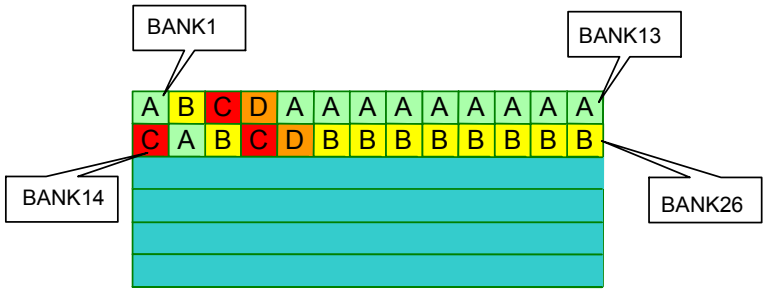
Segment Drivers/Common Drivers

Segment drivers deliver 104 current sources to drive OLED panel. The driving current can be adjusted from 0 to 320uA with 256 steps. Common drivers generate voltage scanning pulses.

Area Colour Decoder

The 104x48 display matrix is divided into six pages. PAGE0 and PAGE1 of the display are divided into 26 banks. Each bank comprises of a display area of 8x8 pixels. Each bank can be programmed to any one of the 4 colours (colour A, B, C, D) as the example shown in Figure 13. Detailed operation can be referred to the Command Table.

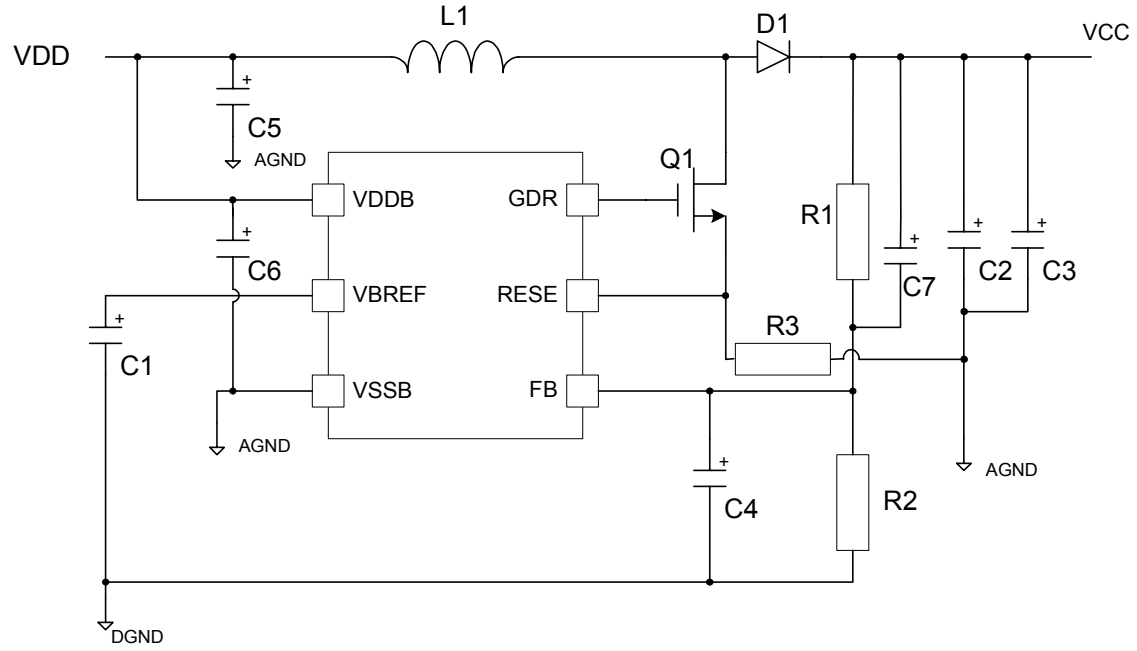
Figure 13 - Example of area color assignment on a 104x48 OLED panel



DC-DC Voltage Converter

It is a switching voltage generator circuit, designed for handheld applications. In SSD0300, internal DC-DC voltage converter accompanying with an external application circuit (shown in below figure) can generate a high voltage supply V_{CC} from a low voltage supply input V_{DD}. V_{CC} is the voltage supply to the OLED driver block. Below application circuit is an example for the input voltage of 3V VDD to generate V_{CC} of 12V @0mA ~ 20mA application.

Figure 14 - DC-DC voltage converter circuit



Remark:

1. VSSB is tied to VSS on SSD0300T3 package.
2. L1, D1, Q1, C5 should be grouped closed together on PCB layout.
3. R1, R2, C1, C4 should be grouped closed together on PCB layout.
4. The VCC output voltage level can be adjusted by R1and R2, the reference formula is:
   VCC = 1.2 x (R1+R2) / R2
   The value of (R1+R2) should be between 500k to 1M Ohm.

Table 3 - Passive component selection:

Components	Typical Value	Remark
L1	Inductor, 10μH	1A
D1	Schottky diode	1A, 25V e.g. 1N5822, BAT54 [Philips Semiconductors]
Q1	MOSFET	N-FET with low R_{DS}(on) and low Vth voltage. e.g. MGSF1N02LT1 [ON SEMI]
R1, R2	Resistor	1%,1/10W
R3	Resistor, 1.2Ω	1%, 1/2W
C1	Capacitor, 1μF	16V
C2	Capacitor, 6.8μF	Low ESR, 25V
C3	Capacitor, 1μF	16V
C4	Capacitor, 10nF	16V
C5	Capacitor, 1 ~ 10 μF	16V
C6	Capacitor, 0.1 ~ 1μF	16V
C7	Capacitor, 15nF	16V

9 COMMAND TABLE

Table 4 - Command table

(D/C =0, R/W(WR#)=0, E(RD#)=1)
Note: commands marked with "**" are compatible to SSD1301

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	00-0F	0	0	0	0	X_3	X_2	X_1	X_0	Set Lower Column Address **	Set the lower nibble of the column address register using $X_3X_2X_1X_0$ as data bits. The initial display line register is reset to 0000b after POR.
0	10-1F	0	0	0	1	X_3	X_2	X_1	X_0	Set Higher Column Address **	Set the higher nibble of the column address register using $X_3X_2X_1X_0$ as data bits. The initial display line register is reset to 0000b after POR.
0	2F	0	0	1	0	1	1	1	1	Activate horizontal scroll	Start horizontal scrolling
0	2E	0	0	1	0	1	1	1	0	Deactivate horizontal scroll	Stop horizontal scrolling
0	26	0	0	1	0	0	1	1	0	Horizontal scroll setup	A[3:0] Set the number of column scroll per step
0	A[3:0]	*	*	*	*	A_3	A_2	A_1	A_0		Valid value: 0001b to 1000b
0	B[2:0]	*	*	*	*	*	B_2	B_1	B_0		B[2:0] Define start page address
0	C[1:0]	*	*	*	*	*	*	C_1	C_0		C[1:0] Set time interval between each scroll step in terms of frame frequency
0	D[2:0]	*	*	*	*	*	D_2	D_1	D_0		00b – 12 frames 01b – 64 frames 10b – 128 frames 11b – 256 frames D[2:0] Define end page address Set the value of D[2:0] larger or equal to B[2:0]
0	40-6F	0	1	X_5	0	X_3	X_2	X_1	X_0	Set Display Start Line	Set display RAM display start line register from 0-47 using $X_5X_3X_2X_1X_0$. Display start line register is reset to 000000 during POR.
0	81	1	0	0	0	0	0	0	1	Set Contrast Control Register **	Double byte command to select 1 out of 256 contrast steps. Contrast increases as the value increases. (POR = 80h)
0	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	91	1	0	0	1	0	0	0	1	Set Look Up Table (LUT) for area colour	Set current drive pulse width of Bank 0, Colour A, B and C.
0	X[5:0]	*	*	X_5	X_4	X_3	X_2	X_1	X_0		
0	A[5:0]	*	*	A_5	A_4	A_3	A_2	A_1	A_0		Bank 0: X[5:0] = 0… 47; for pulse width set to 1 ~ 64 clk
0	B[5:0]	*	*	B_5	B_4	B_3	B_2	B_1	B_0		
0	C[5:0]	*	*	C_5	C_4	C_3	C_2	C_1	C_0		Colour A: A[5:0] same as above Colour B: B[5:0] same as above Colour C: C[5:0] same as above Note: colour D pulse width is fixed at 64 clks pulse.

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	92	1	0	0	1	0	0	1	0	Set bank colour of for bank 1-13 (Page 0)	A[1:0] : 00, 01, 10, or 11 for Colour = A, B, C or D of bank 1 A[3:2] : 00, 01, 10, or 11 for Colour = A, B, C or D of bank 2 : : D[1:0]: 00, 01, 10, or 11 for Colour = A, B, C or D of bank 13
0	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	B[7:0]	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	C[7:0]	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
0	D[1:0]	*	*	*	*	*	*	D_1	D_0		
0	93	1	0	0	1	0	0	1	1	Set bank colour of for bank 14-26 (Page 1)	A[1:0] : 00, 01, 10, or 11 for Colour = A, B, C or D of bank 14 A[3:2] : 00, 01, 10, or 11 for Colour = A, B, C or D of bank 15 : : D[1:0]: 00, 01, 10, or 11 for Colour = A, B, C or D of bank 26
0	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	B[7:0]	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	C[7:0]	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
0	D[1:0]	*	*	*	*	*	*	D_1	D_0		
0	A0~ A1	1	0	1	0	0	0	0	X_0	Set Segment Re-map **	X_0=0:column address 0 is mapped to SEG0 (POR) X_0=1:column address 103 is mapped to SEG0
0	A4~A5	1	0	1	0	0	1	0	X_0	Set Entire Display On/Off **	X_0=0:normal display (POR) X_0=1:entire display on
0	A6~A7	1	0	1	0	0	1	1	X_0	Set Normal/Inverse Display **	X_0=0:normal display (POR) X_0=1:inverse display
0	A8	1	0	1	0	1	0	0	0	Set Multiplex Ratio **	The next command, A[5:0] determines multiplex ratio N from 16MUX-48MUX, POR= 48MUX
0	A[5:0]	*	*	A_5	A_4	A_3	A_2	A_1	A_0		
0	AA	1	0	1	0	1	0	1	0	NOP	Reserved, do not use
0	AB	1	0	1	0	1	0	1	1	NOP	Reserved, do not use
0	AD	1	0	1	0	1	1	0	1	Set DC-DC on/off	X_0 : 1 DC-DC will be turned on when display on (POR) 0 DC-DC is disable X_1=0, Select external VCOMH voltage supply at Display ON X_1=1, Select internal VCOMH regulator at Display ON (POR)
0	A[2:0]	1	0	0	0	1	0	X_1	X_0		
0	AE~AF	1	0	1	0	1	1	1	X_0	Set Display On/Off **	X_0=0:turns off OLED panel (POR) X_0=1:turns on OLED panel
0	B0~B5	1	0	1	1	0	X_2	X_1	X_0	Set Page Address **	Set GDDRAM Page Address (0~5) for read/write using $X_2X_1X_0$
0	C0/C8	1	1	0	0	X_3	*	*	*	Set COM Output Scan Direction **	X_3=0:normal mode (POR) Scan from COM 0 to COM [N –1] X_3=1:remapped mode. Scan from COM [N-1] to COM0 Where N is the Multiplex ratio.

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	D0-D1	1	1	0	1	0	0	0	X_0	Reserved	Reserved, do not use
0 0	D3 A[5:0]	1 *	1 *	0 A_5	1 A_4	0 A_3	0 A_2	1 A_1	1 A_0	Set Display Offset **	Set vertical scroll by COM from 0-47. The value is reset to 00H after POR.
0	D5 A[3:0] A[7:4]	1 * A_7	1 * A_6	0 * A_5	1 * A_4	0 A_3 *	1 A_2 *	0 A_1 *	1 A_0 *	Set Display Clock Divide Ratio/Oscillator Frequency	The lower nibble of the next command sets the divide ratio of the display clocks (dclk). The ratio is the value of A[3:0] +1 Divide ratio= 1-16, POR value is 0000b (divide by 1). The higher nibble of the next command sets the Oscillator Frequency. Oscillator Frequency increases with the value of A[7:4] and vice versa.
0 0	D8	1 0	1 0	0 X_5	1 X_4	1 0	0 X_2	0 0	0 X_0	Set area colour mode on/off & low power display mode	X_5X_4= 00 (POR) : mono mode X_5X_4= 11" Area Colour enable X_2=0 and X_0=0: Normal (POR) power mode X_2=1 and X_0=1: Set low power save mode
0 0	D9 A[7:0]	1 A_7	1 A_6	0 A_5	1 A_4	1 A_3	0 A_2	0 A_1	1 A_0	Set Pre-charge period	A[3:0] Phase 1 period of up to 15 dclk clocks [POR=2h] A[7:4] Phase 2 period of up to 15 dclk clocks [POR=2h]
0 0	DA 02/22	1 0	1 0	0 0	1 X_4	1 0	0 0	1 1	0 0	Set COM pins hardware configuration	X_4=0, Sequential COM pin configuration (i.e. COM23, 22, ….2, 0 ; SEG0-103; COM24,25….46,47) X_4=1(POR), Alternative COM pin configuration (i.e. COM46,44,…2, 0; SEG0 -103; COM1,3,5…,45,47)
0 0	DB A[6:0]	1 *	1 A_6	0 A_5	1 A_4	1 A_3	0 A_2	1 A_1	1 A_0	Set VCOMH	A[6:0] 0000000 0.43*Vref 0111111 0.83*Vref (POR) 1111111 1.0*Vref
0	E2	1	1	1	0	0	0	1	0	Reserved	Reserved
0	E3	1	1	1	0	0	0	1	1	NOP **	Command for No Operation

Note: Remark "*" stands for "Don't Care"

Table 5 - Read command table

(D/C=0, R/W(WR#)=1, E(RD#)=1 for 6800 or E(RD#)=0 for 8080)

Bit Pattern	Command	Description
$D_7D_6D_5D_4D_3D_2D_1D_0$	Status Register Read *	D_7 : "1" for Command lock D_6 : "1" for display OFF / "0" for display ON D_5 : Reserve D_4 : Reserve D_3 : Reserve D_2 : Reserve D_1 : Reserve D_0 : Reserve

Note: Patterns other than that given in Command Table are prohibited to enter to the chip as a command; otherwise, unexpected result will occur.

Data Read / Write

To read data from the GDDRAM, input High to R/W(WR#) pin and D/C# pin for 6800-series parallel mode, Low to E(RD#) pin and High to D/C pin for 8080-series parallel mode. No data read is provided for serial mode.

In normal data read mode, GDDRAM column address pointer will be increased by one automatically after each data read. However, no automatic increase will be performed in read-modify-write mode. Also, a dummy read is required before the first data read. See Figure 8 in Functional Block Description.

To write data to the GDDRAM, input Low to R/W#(WR#) pin and High to D/C# pin for 6800-series parallel mode AND 8080-series parallel mode. For serial interface mode, it is always in write mode. GDDRAM column address pointer will be increased by one automatically after each data write.

Table 6 - Address increment table (Automatic)

D/C#	R/W(WR#)	Comment	Address Increment
0	0	Write Command	No
0	1	Read Status	No
1	0	Write Data	Yes
1	1	Read Data	Yes*1

*1. If read-data command is issued in read-modify-write mode, address increase is not applied.

10 COMMAND DESCRIPTIONS

Set Lower Column Address
This command specifies the lower nibble of the 8-bit column address of the display data RAM. The column address will be incremented by each data access after it is pre-set by the MCU.

Set Higher Column Address
This command specifies the higher nibble of the 8-bit column address of the display data RAM. The column address will be incremented by each data access after it is pre-set by the MCU.

Activate Horizontal Scroll
Start motion of horizontal scrolling. This command should only be issued after Horizontal scroll setup parameters are defined.

The following actions are prohibited after the horizontal scroll is activated

1. RAM access (Data write or read)
2. Changing horizontal scroll setup parameters

The SSD0300 horizontal scroll is designed for 96 columns scrolling only. The 8 remaining columns are reserved for computation during scrolling and should be left open.

Figure 15 - Horizontal scroll direction

Remap Setting	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8	SEG9	SEG10	SEG11	...	...	SEG92	SEG93	SEG94	SEG95	SEG96	SEG97	SEG98	SEG99	SEG100	SEG101	SEG102	SEG103
A0	A	B	C	D	E	F	G	H	I	J	K	L	→	→	W	X	Y	Z	Invalid data							
A1	Invalid data								Z	Y	X	W	←	←	L	K	J	I	H	G	F	E	D	C	B	A

Scroll direction

Deactivate Horizontal Scroll
Stop motion of horizontal scrolling.

Horizontal Scroll Setup
This command consists of 5 consecutive bytes to set up the horizontal scroll parameters. It determines scroll direction, scrolling start page, end page and scrolling speed.

Before issuing this command, the horizontal scroll must be deactivated (2Fh). Otherwise, ram content may be corrupted.

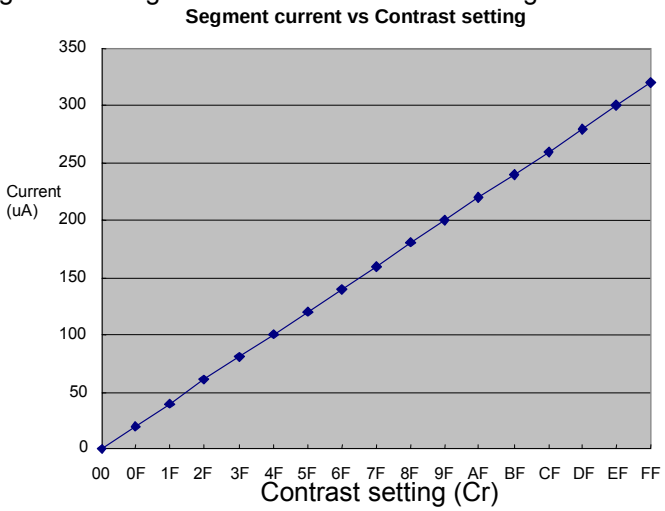
Set Display Start Line

This command is to set Display Start Line register to determine starting address of display RAM to be displayed by selecting a value from 0 to 47. With value equals to 0, D_0 of Page 0 is mapped to COM0. With value equals to 1, D_1 of Page0 is mapped to COM0. The display start line values of 0 to 47 are assigned to Page 0 to 7.

Set Contrast Control Register

This command is to set Contrast Setting of the display. The chip has 256 contrast steps from 00 to FF. The segment output current increases as the contrast step value increases. See Figure 6 below.

Figure 16 - Segment current vs Contrast setting



Segment output current setting:

Iseg = Cr/256 * Iref * scale factor

Where:
Cr is contrast step
Iref is reference current equals 10uA
Scale factor =32

Set Look Up Table (LUT) for area colour

SSD0300 provides 4 colour (pulse width) settings - Colour A, B, C and D. The colour intensity (or grey scale) is defined by the current drive pulse width. The pulse width of colour A, B, C can be programmable from 1 to 64 DCLK* duration. The colour D is fixed at 64 DCLK pulse width. This colour setting has to be stored in the Look Up Table (LUT).

For the background colour, the colour intensity is defined by a variable X[5:0].

Set LUT command: 10010001
X[5:0]
A[5:0]
B[5:0]
C[5:0]

	Description	Number of DCLKs
Bank 0	Set background colour	X[5:0]
Colour A	Set Pulse Width A	A[5:0]
Colour B	Set Pulse Width B	B[5:0]
Colour C	Set Pulse Width C	C[5:0]
Colour D	Pulse width D is fixed to 64 DCLK	64 (fixed)

DCLK: Internal Display Clock

Set bank colour of bank 1-13 (Page 0) and bank colour of bank 14-26 (Page 1)

Next step is to define the colour of each display area. The 104x48 display matrix is divided into 8 pages of 8 commons per pages. The first two pages, page 0 and page 1, are divided into 32 banks: Each bank comprise of a display area of 8x8 pixels. Each bank can be programmable to any 1 of the 4 colour (A, B, C, D). User can use 92h and 93h command for the bank colour setting. Note: Only applicable in colour mode.

Set Segment Re-map
This command changes the mapping between the display data column address and segment driver. It allows flexibility in OLED module design. Refer to Command Table.

Set Entire Display On/Off
This command forces the entire display to be "ON" regardless of the contents of the display data RAM. This command has priority over normal/reverse display. This command will be used with "Set Display ON/OFF" command to form a compound command for entering power save mode.

Set Normal/Inverse Display
This command sets the display to be either normal/inverse. In normal display, a RAM data of 1 indicates an "ON" pixel while in inverse display; a RAM data of 0 indicates an "ON" pixel.

Set Multiplex Ratio
This command switches default 47 multiplex mode to any multiplex ratio from 2 to 47. The output pads COM0-COM47 will be switched to corresponding COM signal.

Set Display On/Off
This command turns the display on or off. When the display is off, the segment and common output are in high impedance state.

Set Page Address
This command positions the page address from 0 to 5 in GDDRAM. Refer to Command Table.

Set COM Output Scan Direction
This command sets the scan direction of the COM output allowing layout flexibility in OLED module design. In addition, the display will have immediate effect once this command is issued. That is, if this command is sent during normal display, the graphic display will be vertically flipped.

Set Display Offset

This is a double byte command. The next command specifies the mapping of display start line (it is assumed that COM0 is the display start line, display start line register equals to 0) to one of COM0-47.

For example, to move the COM16 towards the COM0 direction for 16 lines, the 6-bit data in the second byte should be given by 010000. To move in the opposite direction by 16 lines, the 6-bit data should be given by (48 – 16) and so the second byte should be 100000.

	Output													
	48		48		48		40		40		40		32	Set MUX ratio(A8)
	Remap		Remap		Remap		Remap		Remap		Remap		Remap	COM Normal / Remapped (C0 / C8)
Hardware	0		8		0		0		8		0		8	Display offset (D3)
pin name	0		0		8		0		0		8		16	Display start line (40 - 7F)
COM0	Row47	Ram47	Row7	Ram7	Row47	Ram7	-	-	Row7	Ram7	-	-	Row7	Ram23
COM1	Row46	Ram46	Row6	Ram6	Row46	Ram6	-	-	Row6	Ram6	-	-	Row6	Ram22
COM2	Row45	Ram45	Row5	Ram5	Row45	Ram5	-	-	Row5	Ram5	-	-	Row5	Ram21
COM3	Row44	Ram44	Row4	Ram4	Row44	Ram4	-	-	Row4	Ram4	-	-	Row4	Ram20
COM4	Row43	Ram43	Row3	Ram3	Row43	Ram3	-	-	Row3	Ram3	-	-	Row3	Ram19
COM5	Row42	Ram42	Row2	Ram2	Row42	Ram2	-	-	Row2	Ram2	-	-	Row2	Ram18
COM6	Row41	Ram41	Row1	Ram1	Row41	Ram1	-	-	Row1	Ram1	-	-	Row1	Ram17
COM7	Row40	Ram40	Row0	Ram0	Row40	Ram0	-	-	Row0	Ram0	-	-	Row0	Ram16
COM8	Row39	Ram39	Row47	Ram47	Row39	Ram47	Row39	RAM39	-	-	Row39	RAM47	-	-
COM9	Row38	Ram38	Row46	Ram46	Row38	Ram46	Row38	RAM38	-	-	Row38	RAM46	-	-
COM10	Row37	Ram37	Row45	Ram45	Row37	Ram45	Row37	RAM37	-	-	Row37	RAM45	-	-
COM11	Row36	Ram36	Row44	Ram44	Row36	Ram44	Row36	RAM36	-	-	Row36	RAM44	-	-
COM12	Row35	Ram35	Row43	Ram43	Row35	Ram43	Row35	RAM35	-	-	Row35	RAM43	-	-
COM13	Row34	Ram34	Row42	Ram42	Row34	Ram42	Row34	RAM34	-	-	Row34	RAM42	-	-
COM14	Row33	Ram33	Row41	Ram41	Row33	Ram41	Row33	RAM33	-	-	Row33	RAM41	-	-
COM15	Row32	Ram32	Row40	Ram40	Row32	Ram40	Row32	RAM32	-	-	Row32	RAM40	-	-
COM16	Row31	Ram31	Row39	Ram39	Row31	Ram39	Row31	RAM31	Row39	RAM39	Row31	RAM39	-	-
COM17	Row30	Ram30	Row38	Ram38	Row30	Ram38	Row30	RAM30	Row38	RAM38	Row30	RAM38	-	-
COM18	Row29	Ram29	Row37	Ram37	Row29	Ram37	Row29	RAM29	Row37	RAM37	Row29	RAM37	-	-
COM19	Row28	Ram28	Row36	Ram36	Row28	Ram36	Row28	RAM28	Row36	RAM36	Row28	RAM36	-	-
COM20	Row27	Ram27	Row35	Ram35	Row27	Ram35	Row27	RAM27	Row35	RAM35	Row27	RAM35	-	-
COM21	Row26	Ram26	Row34	Ram34	Row26	Ram34	Row26	RAM26	Row34	RAM34	Row26	RAM34	-	-
COM22	Row25	Ram25	Row33	Ram33	Row25	Ram33	Row25	RAM25	Row33	RAM33	Row25	RAM33	-	-
COM23	Row24	Ram24	Row32	Ram32	Row24	Ram32	Row24	RAM24	Row32	RAM32	Row24	RAM32	-	-
COM24	Row23	Ram23	Row31	Ram31	Row23	Ram31	Row23	RAM23	Row31	RAM31	Row23	RAM31	Row31	RAM47
COM25	Row22	Ram22	Row30	Ram30	Row22	Ram30	Row22	RAM22	Row30	RAM30	Row22	RAM30	Row30	RAM46
COM26	Row21	Ram21	Row29	Ram29	Row21	Ram29	Row21	RAM21	Row29	RAM29	Row21	RAM29	Row29	RAM45
COM27	Row20	Ram20	Row28	Ram28	Row20	Ram28	Row20	RAM20	Row28	RAM28	Row20	RAM28	Row28	RAM44
COM28	Row19	Ram19	Row27	Ram27	Row19	Ram27	Row19	RAM19	Row27	RAM27	Row19	RAM27	Row27	RAM43
COM29	Row18	Ram18	Row26	Ram26	Row18	Ram26	Row18	RAM18	Row26	RAM26	Row18	RAM26	Row26	RAM42
COM30	Row17	Ram17	Row25	Ram25	Row17	Ram25	Row17	RAM17	Row25	RAM25	Row17	RAM25	Row25	RAM41
COM31	Row16	Ram16	Row24	Ram24	Row16	Ram24	Row16	RAM16	Row24	RAM24	Row16	RAM24	Row24	RAM40
COM32	Row15	Ram15	Row23	Ram23	Row15	Ram23	Row15	RAM15	Row23	RAM23	Row15	RAM23	Row23	RAM39
COM33	Row14	Ram14	Row22	Ram22	Row14	Ram22	Row14	RAM14	Row22	RAM22	Row14	RAM22	Row22	RAM38
COM34	Row13	Ram13	Row21	Ram21	Row13	Ram21	Row13	RAM13	Row21	RAM21	Row13	RAM21	Row21	RAM37
COM35	Row12	Ram12	Row20	Ram20	Row12	Ram20	Row12	RAM12	Row20	RAM20	Row12	RAM20	Row20	RAM36
COM36	Row11	Ram11	Row19	Ram19	Row11	Ram19	Row11	RAM11	Row19	RAM19	Row11	RAM19	Row19	RAM35
COM37	Row10	Ram10	Row18	Ram18	Row10	Ram18	Row10	RAM10	Row18	RAM18	Row10	RAM18	Row18	RAM34
COM38	Row9	Ram9	Row17	Ram17	Row9	Ram17	Row9	RAM9	Row17	RAM17	Row9	RAM17	Row17	RAM33
COM39	Row8	Ram8	Row16	Ram16	Row8	Ram16	Row8	RAM8	Row16	RAM16	Row8	RAM16	Row16	RAM32
COM40	Row7	Ram7	Row15	Ram15	Row7	Ram15	Row7	RAM7	Row15	RAM15	Row7	RAM15	Row15	RAM31
COM41	Row6	Ram6	Row14	Ram14	Row6	Ram14	Row6	RAM6	Row14	RAM14	Row6	RAM14	Row14	RAM30
COM42	Row5	Ram5	Row13	Ram13	Row5	Ram13	Row5	RAM5	Row13	RAM13	Row5	RAM13	Row13	RAM29
COM43	Row4	Ram4	Row12	Ram12	Row4	Ram12	Row4	RAM4	Row12	RAM12	Row4	RAM12	Row12	RAM28
COM44	Row3	Ram3	Row11	Ram11	Row3	Ram11	Row3	RAM3	Row11	RAM11	Row3	RAM11	Row11	RAM27
COM45	Row2	Ram2	Row10	Ram10	Row2	Ram10	Row2	RAM2	Row10	RAM10	Row2	RAM10	Row10	RAM26
COM46	Row1	Ram1	Row9	Ram9	Row1	Ram9	Row1	RAM1	Row9	RAM9	Row1	RAM9	Row9	RAM25
COM47	Row0	Ram0	Row8	Ram8	Row0	Ram8	Row0	RAM0	Row8	RAM8	Row0	RAM8	Row8	RAM24

	Output												
	48		48		48		40		40		40		Set MUX ratio(A8)
	Normal		Normal		Normal		Normal		Normal		Normal		COM Normal / Remapped (C0 / C8)
Hardware	0		8		0		0		8		0		Display offset (D3)
pin name	0		0		8		0		0		8		Display start line (40 - 7F)
COM0	Row0	RAM0	Row8	RAM8	Row0	RAM8	Row0	RAM0	Row8	RAM8	Row0	RAM8	
COM1	Row1	RAM1	Row9	RAM9	Row1	RAM9	Row1	RAM1	Row9	RAM9	Row1	RAM9	
COM2	Row2	RAM2	Row10	RAM10	Row2	RAM10	Row2	RAM2	Row10	RAM10	Row2	RAM10	
COM3	Row3	RAM3	Row11	RAM11	Row3	RAM11	Row3	RAM3	Row11	RAM11	Row3	RAM11	
COM4	Row4	RAM4	Row12	RAM12	Row4	RAM12	Row4	RAM4	Row12	RAM12	Row4	RAM12	
COM5	Row5	RAM5	Row13	RAM13	Row5	RAM13	Row5	RAM5	Row13	RAM13	Row5	RAM13	
COM6	Row6	RAM6	Row14	RAM14	Row6	RAM14	Row6	RAM6	Row14	RAM14	Row6	RAM14	
COM7	Row7	RAM7	Row15	RAM15	Row7	RAM15	Row7	RAM7	Row15	RAM15	Row7	RAM15	
COM8	Row8	RAM8	Row16	RAM16	Row8	RAM16	Row8	RAM8	Row16	RAM16	Row8	RAM16	
COM9	Row9	RAM9	Row17	RAM17	Row9	RAM17	Row9	RAM9	Row17	RAM17	Row9	RAM17	
COM10	Row10	RAM10	Row18	RAM18	Row10	RAM18	Row10	RAM10	Row18	RAM18	Row10	RAM18	
COM11	Row11	RAM11	Row19	RAM19	Row11	RAM19	Row11	RAM11	Row19	RAM19	Row11	RAM19	
COM12	Row12	RAM12	Row20	RAM20	Row12	RAM20	Row12	RAM12	Row20	RAM20	Row12	RAM20	
COM13	Row13	RAM13	Row21	RAM21	Row13	RAM21	Row13	RAM13	Row21	RAM21	Row13	RAM21	
COM14	Row14	RAM14	Row22	RAM22	Row14	RAM22	Row14	RAM14	Row22	RAM22	Row14	RAM22	
COM15	Row15	RAM15	Row23	RAM23	Row15	RAM23	Row15	RAM15	Row23	RAM23	Row15	RAM23	
COM16	Row16	RAM16	Row24	RAM24	Row16	RAM24	Row16	RAM16	Row24	RAM24	Row16	RAM24	
COM17	Row17	RAM17	Row25	RAM25	Row17	RAM25	Row17	RAM17	Row25	RAM25	Row17	RAM25	
COM18	Row18	RAM18	Row26	RAM26	Row18	RAM26	Row18	RAM18	Row26	RAM26	Row18	RAM26	
COM19	Row19	RAM19	Row27	RAM27	Row19	RAM27	Row19	RAM19	Row27	RAM27	Row19	RAM27	
COM20	Row20	RAM20	Row28	RAM28	Row20	RAM28	Row20	RAM20	Row28	RAM28	Row20	RAM28	
COM21	Row21	RAM21	Row29	RAM29	Row21	RAM29	Row21	RAM21	Row29	RAM29	Row21	RAM29	
COM22	Row22	RAM22	Row30	RAM30	Row22	RAM30	Row22	RAM22	Row30	RAM30	Row22	RAM30	
COM23	Row23	RAM23	Row31	RAM31	Row23	RAM31	Row23	RAM23	Row31	RAM31	Row23	RAM31	
COM24	Row24	RAM24	Row32	RAM32	Row24	RAM32	Row24	RAM24	Row32	RAM32	Row24	RAM32	
COM25	Row25	RAM25	Row33	RAM33	Row25	RAM33	Row25	RAM25	Row33	RAM33	Row25	RAM33	
COM26	Row26	RAM26	Row34	RAM34	Row26	RAM34	Row26	RAM26	Row34	RAM34	Row26	RAM34	
COM27	Row27	RAM27	Row35	RAM35	Row27	RAM35	Row27	RAM27	Row35	RAM35	Row27	RAM35	
COM28	Row28	RAM28	Row36	RAM36	Row28	RAM36	Row28	RAM28	Row36	RAM36	Row28	RAM36	
COM29	Row29	RAM29	Row37	RAM37	Row29	RAM37	Row29	RAM29	Row37	RAM37	Row29	RAM37	
COM30	Row30	RAM30	Row38	RAM38	Row30	RAM38	Row30	RAM30	Row38	RAM38	Row30	RAM38	
COM31	Row31	RAM31	Row39	RAM39	Row31	RAM39	Row31	RAM31	Row39	RAM39	Row31	RAM39	
COM32	Row32	RAM32	Row40	RAM40	Row32	RAM40	Row32	RAM32	-	-	Row32	RAM40	
COM33	Row33	RAM33	Row41	RAM41	Row33	RAM41	Row33	RAM33	-	-	Row33	RAM41	
COM34	Row34	RAM34	Row42	RAM42	Row34	RAM42	Row34	RAM34	-	-	Row34	RAM42	
COM35	Row35	RAM35	Row43	RAM43	Row35	RAM43	Row35	RAM35	-	-	Row35	RAM43	
COM36	Row36	RAM36	Row44	RAM44	Row36	RAM44	Row36	RAM36	-	-	Row36	RAM44	
COM37	Row37	RAM37	Row45	RAM45	Row37	RAM45	Row37	RAM37	-	-	Row37	RAM45	
COM38	Row38	RAM38	Row46	RAM46	Row38	RAM46	Row38	RAM38	-	-	Row38	RAM46	
COM39	Row39	RAM39	Row47	RAM47	Row39	RAM47	Row39	RAM39	-	-	Row39	RAM47	
COM40	Row40	RAM40	Row0	RAM0	Row40	RAM48	-	-	Row0	RAM0	-	-	
COM41	Row41	RAM41	Row1	RAM1	Row41	RAM49	-	-	Row1	RAM1	-	-	
COM42	Row42	RAM42	Row2	RAM2	Row42	RAM50	-	-	Row2	RAM2	-	-	
COM43	Row43	RAM43	Row3	RAM3	Row43	RAM51	-	-	Row3	RAM3	-	-	
COM44	Row44	RAM44	Row4	RAM4	Row44	RAM52	-	-	Row4	RAM4	-	-	
COM45	Row45	RAM45	Row5	RAM5	Row45	RAM53	-	-	Row5	RAM5	-	-	
COM46	Row46	RAM46	Row6	RAM6	Row46	RAM54	-	-	Row6	RAM6	-	-	
COM47	Row47	RAM47	Row7	RAM7	Row47	RAM55	-	-	Row7	RAM7	-	-	

Set Display Clock Divide Ratio/ Oscillator Frequency

This command is used to set the frequency of the internal display clocks, DCLKs. It is defined as the divide ratio (Value from 1 to 16) used to divide the oscillator frequency. POR is 0000b which means the divide ratio is 1. Frame frequency is determined by divide ratio, number of display clocks per row, MUX ratio and oscillator frequency.

Set Area Colour Mode on/off

This command is used to enable area colour mode. POR is mono mode.

Set Low Power Display Mode

This is a double byte command. This command is set to reduce power consumption during IC operation.

Set Pre-charge period

This command is used to set the duration of the pre-charge period. The interval is counted in number of DCLK. POR is 2 DCLK.

Set COM pins hardware configuration
This command is to set the COM signals pin configuration (sequential or alternative) to match the OLED panel hardware layout

Alternative COM pin configuration (POR):

COM46, 44, 42…0	**SEG0, 1, 2… 103**	**COM1, 3, 5…47**

Sequential COM pin configuration:

COM23, 22, 21…0	**SEG0, 1, 2… 103**	**COM24, 25, 26…47**

NOP
No Operation Command

Status register Read
This command is issued by setting D/C# Low during a data read (refer to Figure 8 and Figure 9 parallel interface waveform). It allows the MCU to monitor the internal status of the chip. No status read is provided for serial mode.

Set DC-DC on/off
This command is to control the DC-DC voltage converter. The converter will be turned on by issuing this command then DISPLAY ON command. The panel display must be off while issuing this command. POR the DC-DC will be turned on.

Set V_{COMH} Voltage
This command sets the high voltage level of common pins, V_{COMH}, when it is selected to generate internally by command ADh. The level of V_{COMH} is programmed with reference to V_{REF}.

11 MAXIMUM RATINGS

Table 7 - Maximum Ratings (Voltage Reference to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to +4.0	V
V_{CC}		0.0 to 18.0	V
V_{REF}		0.0 to 18.0	V
V_{COMH}	Supply Voltage/Output voltage	0.0 to 18.0	V
-	SEG/COM output voltage	0.0 to 18.0	V
V_{in}	Input voltage	Vss-0.3 to Vdd+0.3	V
T_A	Operating Temperature	-40 to +85	ºC
T_{stg}	Storage Temperature Range	-65 to +150	ºC

Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description.

12 DC CHARACTERISTICS

Table 8 - DC Characteristics

(Unless otherwise specified, Voltage Referenced to V_{SS}, V_{DD} = 2.4 to 3.5V, T_A = 25°C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{CC}	Operating Voltage	-	7	12	16	V
V_{DD}	Logic Supply Voltage	-	2.4	-	3.5	V
V_{DD}	Logic Supply Voltage (internal DC/DC enable)	-	3.0	-	3.5	V
V_{OH}	High Logic Output Level	I_{OUT} = 100uA, 3.3MHz	0.9*V_{DD}	-	V_{DD}	V
V_{OL}	Low Logic Output Level	I_{OUT} = 100uA, 3.3MHz	0	-	0.1*V_{DD}	V
V_{IH}	High Logic Input Level	I_{OUT} = 100uA, 3.3MHz	0.8*V_{DD}	-	V_{DD}	V
V_{IL}	Low Logic Input Level	I_{OUT} = 100uA, 3.3MHz	0	-	0.2*V_{DD}	V
$I_{CC, SLEEP}$	Sleep mode Current	V_{DD}=2.7V, display OFF, No panel attached	-15	-	+15	uA
$I_{DD, SLEEP}$	Sleep mode Current	V_{DD}=2.7V, display OFF, No panel attached	-15	-	+15	uA
I_{CC}	V_{CC} Supply Current	Contrast = FF	-	550	-	uA
I_{DD}	V_{DD} Supply Current	Contrast = FF	-	190	-	uA
I_{SEG}	Segment Output Current V_{DD}=2.7V, V_{CC}=12V, I_{REF}=10uA, Display on, Segment pin under test is connected with a 20K resistive load to V_{SS}	Contrast=FF	285	320	355	uA
		Contrast=AF	-	220	-	
		Contrast=5F	-	120	-	
		Contrast=0F	-	20	-	
Dev	Segment output current uniformity	Dev = (I_{SEG} – I_{MID})/I_{MID} I_{MID} = (I_{MAX} + I_{MIN})/2 I_{SEG}[0:103] = Segment current at contrast = FF	-	-	±3	%
Adj. Dev	Adjacent pin output current uniformity (contrast = FF)	Adj Dev = (I[n]-I[n+1]) / (I[n]+I[n+1])	-	±2.0	--	%
Vcc	DC-DC converter output voltage	V_{DD} input=3V, L=10uH; R1=450Kohm; R2=50Kohm; Icc = 20mA(loading)	11.0	12.0	13.0	V
		-	7	-	16	
Pwr	DC-DC Converter output power	V_{DD} input=3V, L=10uH; V_{CC}= 12V	-	-	400	mW

13 AC CHARACTERISTICS

Table 9 - AC Characteristics

(Unless otherwise specified, Voltage Referenced to V_{SS}, V_{DD} = 2.4 to 3.5V, T_A = 25°C.)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
F_{OSC}	Oscillation Frequency of Display Timing Generator	V_{DD} = 2.7V	260	280	310	kHz
F_{FRM}	Frame Frequency for 48 MUX Mode	104x48 Graphic Display Mode, Display ON, Internal Oscillator Enabled	-	F_{OSC} X 1/(D*K*48)	-	Hz

D: divide ratio (default value = 1)
K: number of display clocks (default value = 54)
Refer to command table for detail description

14 Timing characteristics

Table 10 - I^2C Interface Timing Characteristics (V_{DD}-V_{SS}=2.4 to 3.5V, T_A=-40 to 85° C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	-	us
t_{HSTART}	Start condition Hold Time	0.6	-	-	us
t_{HD}	Data Hold Time	300	-	-	ns
t_{SD}	Data Setup Time	100	-	-	ns
t_{SSTART}	Start condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	-	us
t_{SSTOP}	Stop condition Setup Time	0.6	-	-	us
t_R	Rise Time for data and clock pin	-	-	300	ns
t_F	Fall Time for data and clock pin	-	-	300	ns
t_{IDLE}	Idle Time before a new transmission can start	1.3	-	-	us

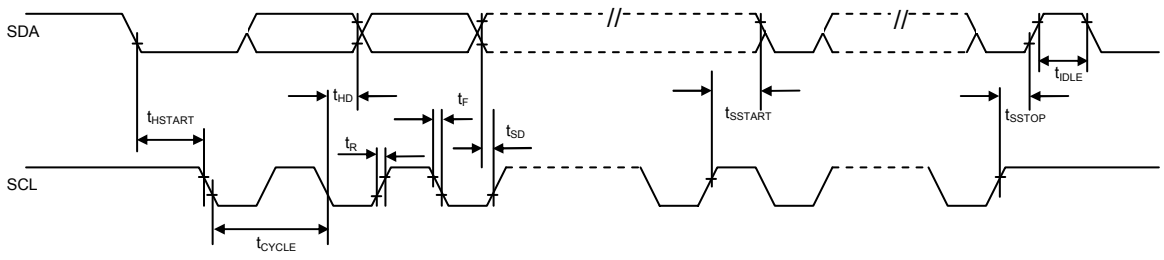


Figure 17 - I^2C interface characteristics

Table 11 - 6800-Series MPU Parallel Interface Timing Characteristics

(V_{DD} - V_{SS} = 2.4 to 3.5V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

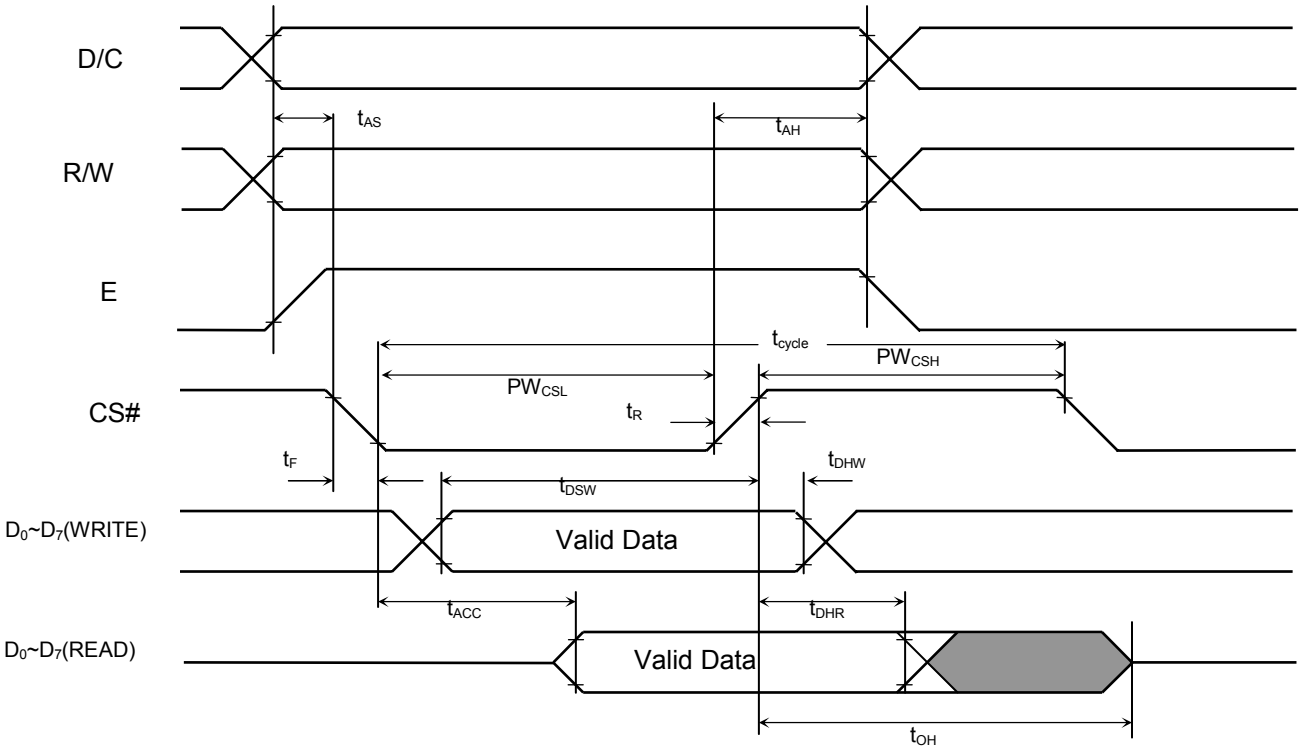


Figure 18 - 6800-series MPU parallel interface characteristics

Table 12 - 8080-Series MPU Parallel Interface Timing Characteristics

(V_{DD} - V_{SS} = 2.4 to 3.5V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

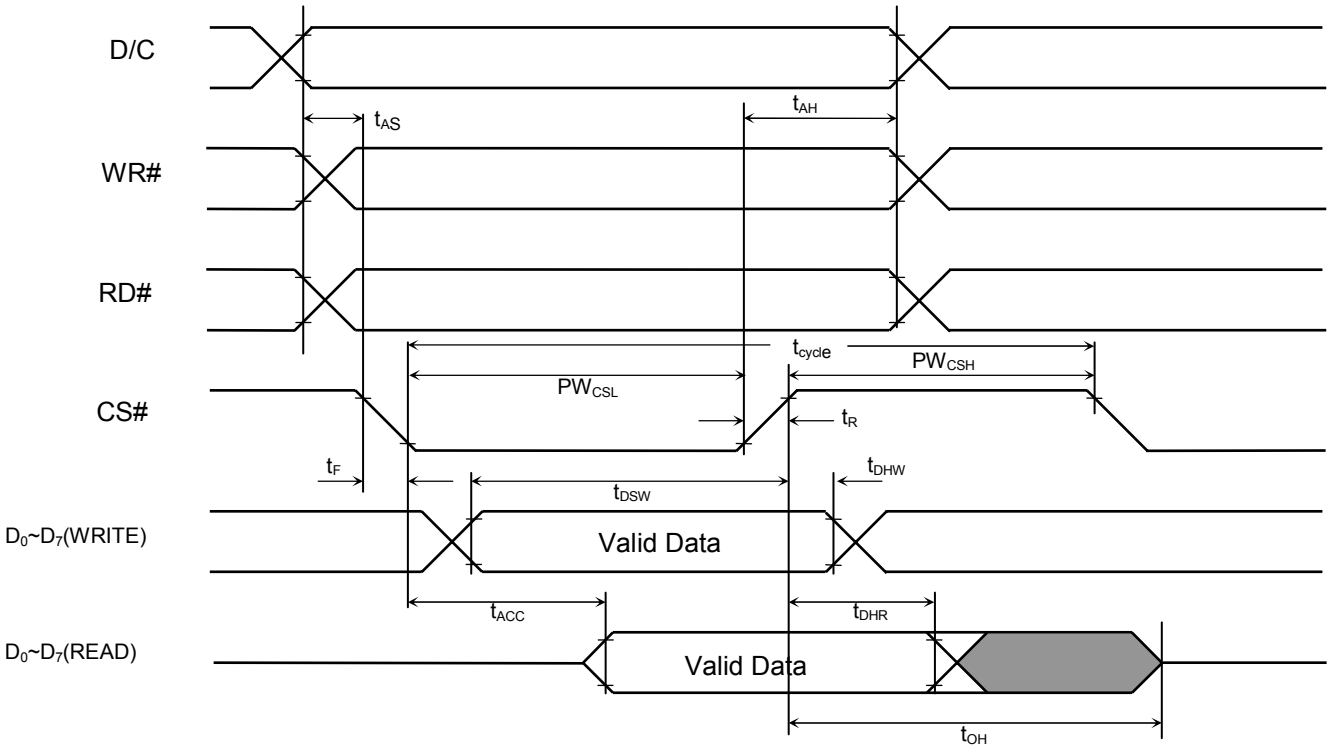


Figure 19 - 8080-series MPU parallel interface characteristics

Table 13 - Serial Interface Timing Characteristics

(V_{DD} - V_{SS} = 2.4 to 3.5V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	-	ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150	-	-	ns
t_{CSS}	Chip Select Setup Time	120	-	-	ns
t_{CSH}	Chip Select Hold Time	60	-	-	ns
t_{DSW}	Write Data Setup Time	100	-	-	ns
t_{DHW}	Write Data Hold Time	100	-	-	ns
t_{CLKL}	Clock Low Time	100	-	-	ns
t_{CLKH}	Clock High Time	100	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

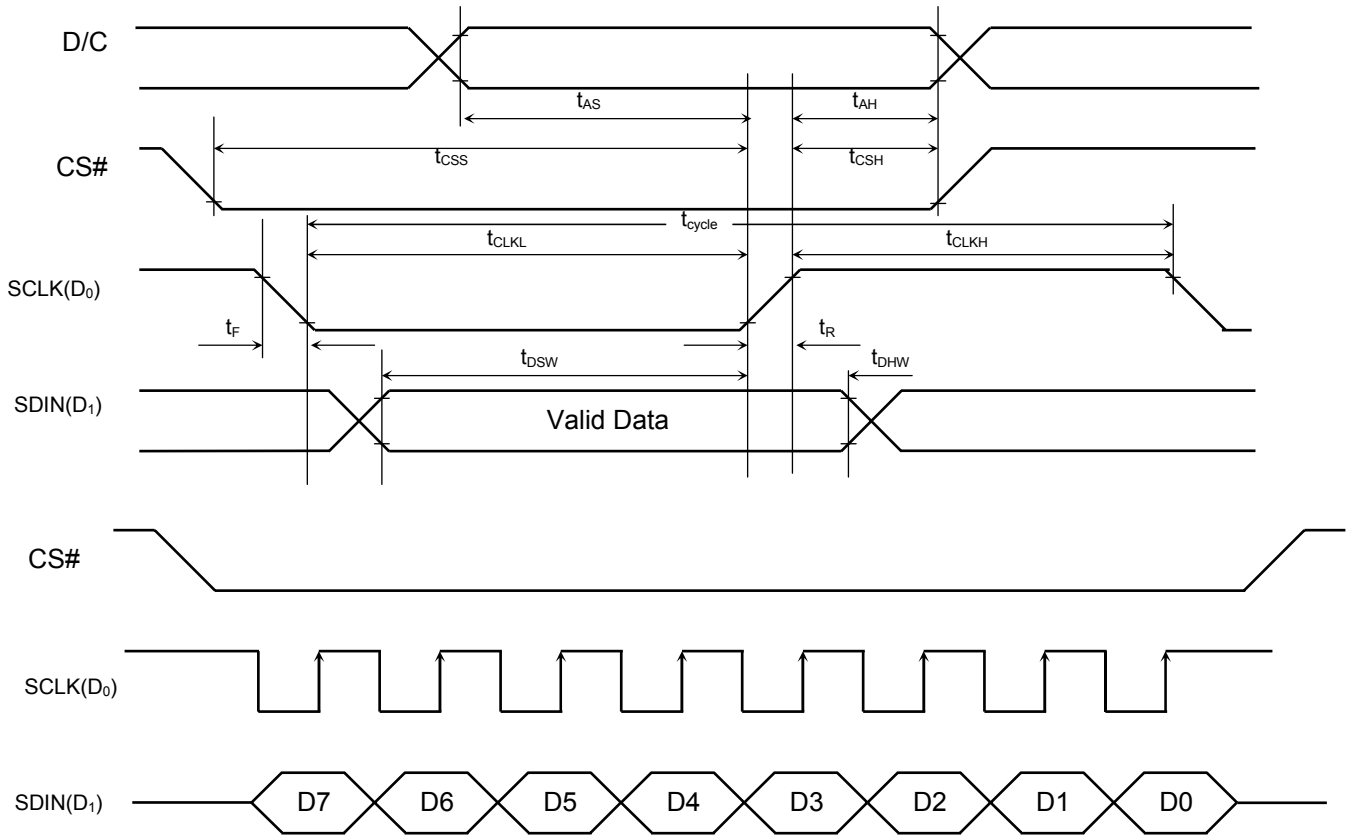
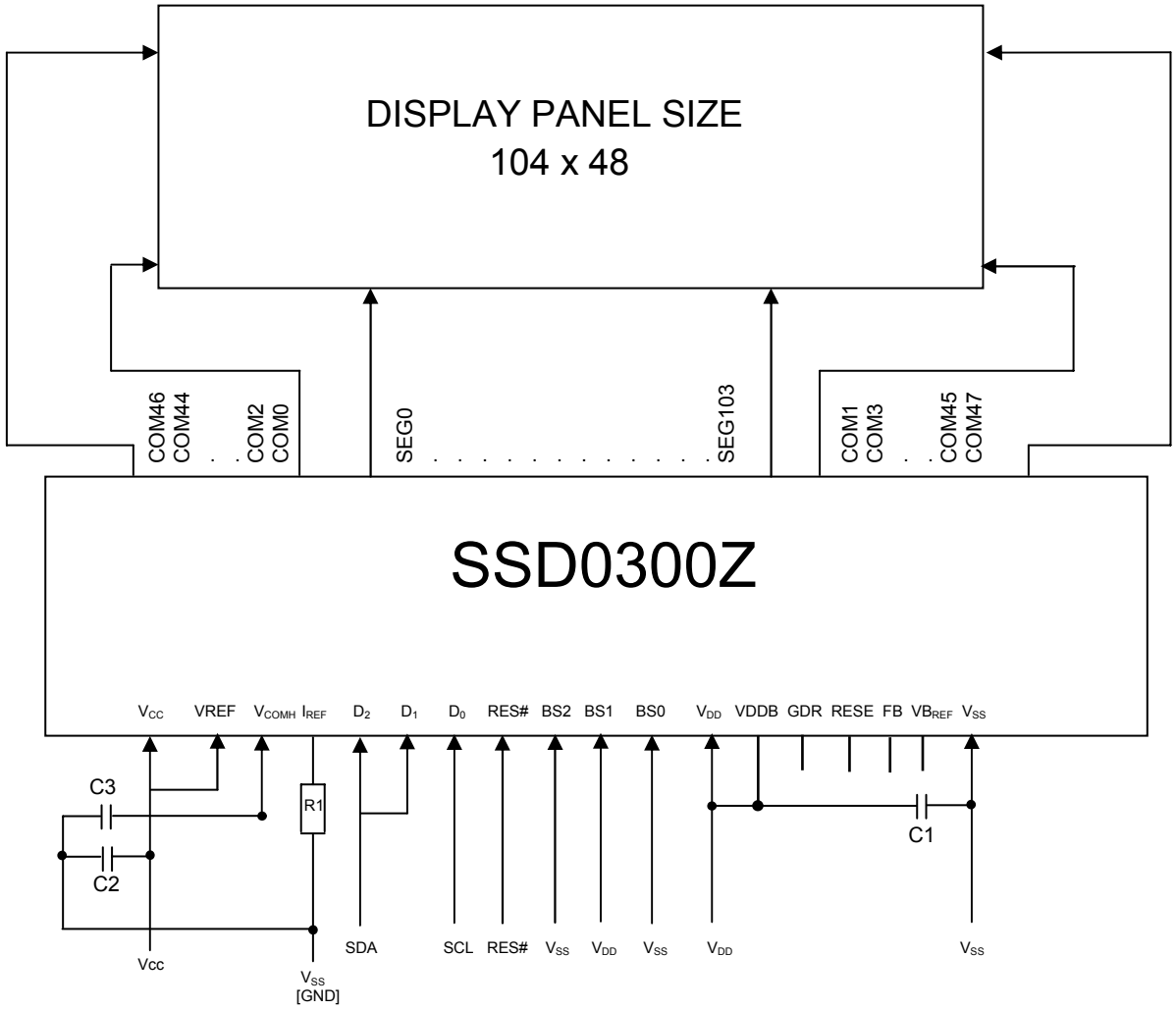


Figure 20 - Serial interface characteristics

15 APPLICATION EXAMPLE

Figure 21 - Application example for SSD0300

The typical configuration for I^2C interface mode & externally V_{CC} are shown in the following diagram:
(V_{DD}=2.7V, V_{CC}=V_{REF}=12V, I_{REF}=10uA



Pin externally connected to VSS: VSSB, BGGND
D/C# (SA0): Tie to HIGH or LOW for address selection
CLS – Tie to HIGH for internal oscillator
D_3 – D_7, R/W# (RW#), E (RD#), CS#: Tie to LOW
CL, GDR, RESE, VB_{REF}, FB should be left open individually
VCL, VSL: connect to V_{SS} to ground;

C1~ C3: 4.7uF
R1: 910kΩ, R1=(Voltage at IREF pin-VSS)/I_{REF}
Voltage at IREF pin = VCC-3V

16 SSD0300TR1 TAB Package

SSD0300TR1 pin assignment

Figure 22 - SSD0300TR1 pin assignment

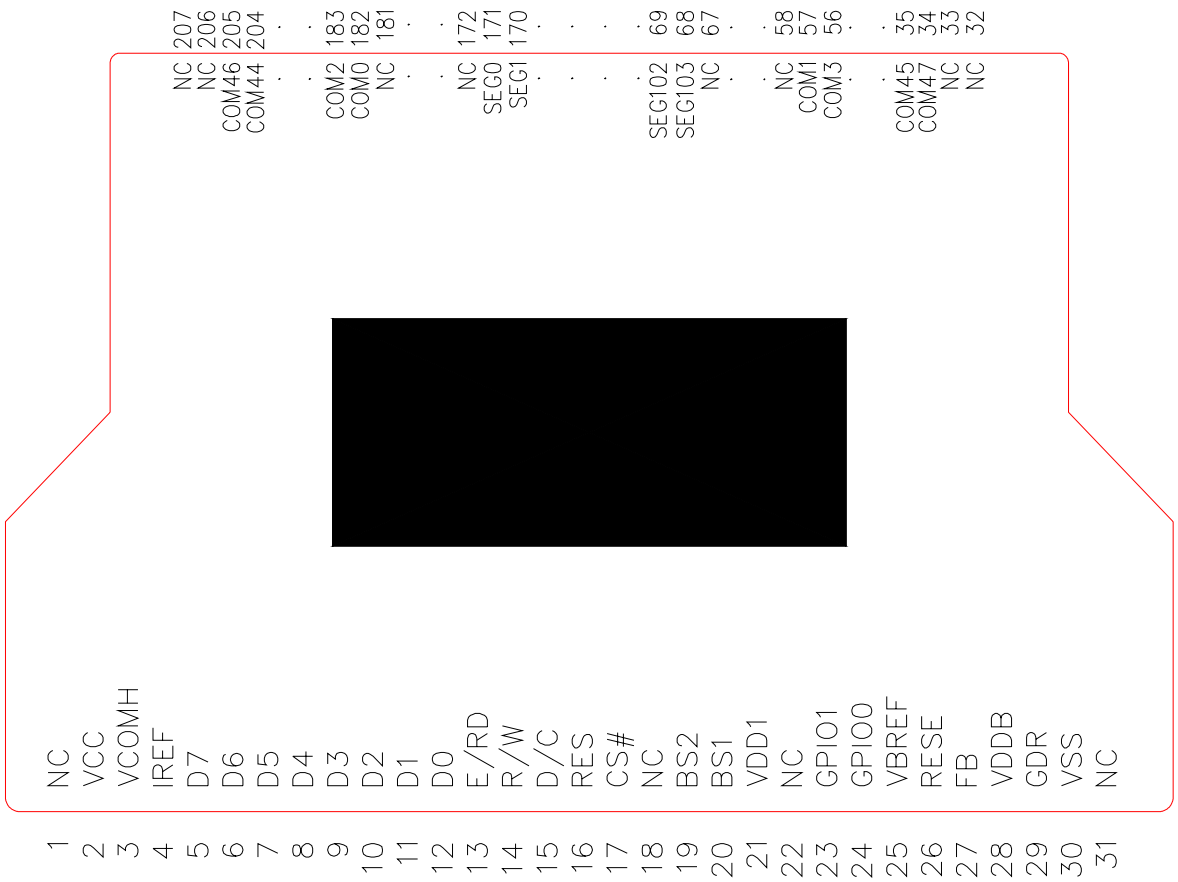


Table 14 - SSD0300TR1 pin assignment

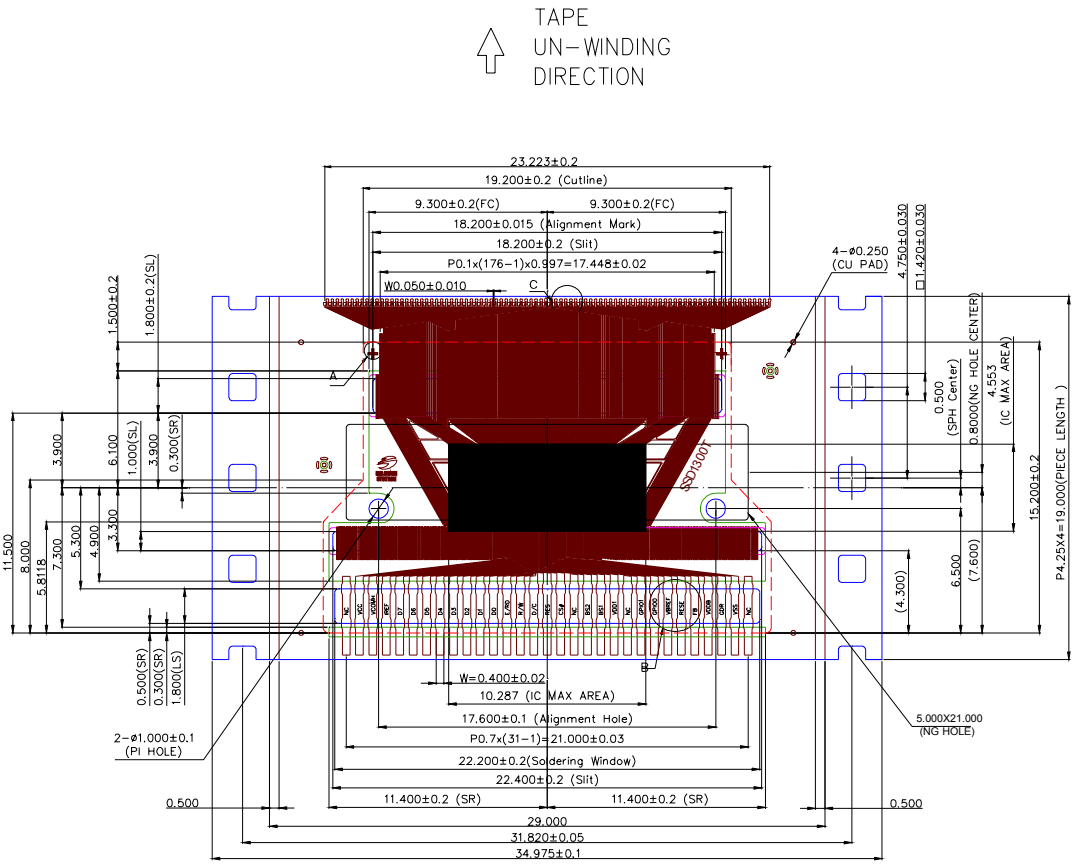
Pin no.	Pin Name
1	NC
2	VCC
3	VCOMH
4	IREF
5	D7
6	D6
7	D5
8	D4
9	D3
10	D2
11	D1
12	D0
13	E
14	R/W
15	D/C
16	RES#
17	CS#
18	NC
19	BS2
20	BS1
21	VDD1
22	NC
23	GPIO1
24	GPIO0
25	VBREF
26	RESE
27	FB
28	VDDB
29	GDR
30	VSS
31	NC
32	NC
33	NC
34	COM47
35	COM45
36	COM43
37	COM41
38	COM39
39	COM37
40	COM35
41	COM33
42	COM31
43	COM29
44	COM27
45	COM25
46	COM23
47	COM21
48	COM19
49	COM17
50	COM15
51	COM13
52	COM11
53	COM9
54	COM7
55	COM5
56	COM3
57	COM1
58	NC
59	NC
60	NC
61	NC
62	NC
63	NC
64	NC
65	NC
66	NC
67	NC
68	SEG103
69	SEG102
70	SEG101
71	SEG100
72	SEG99
73	SEG98
74	SEG97
75	SEG96
76	SEG95
77	SEG94
78	SEG93
79	SEG92
80	SEG91

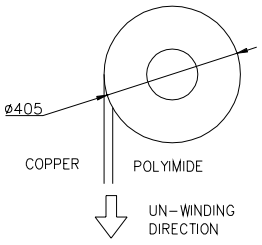
Pin no.	Pin Name
81	SEG90
82	SEG89
83	SEG88
84	SEG87
85	SEG86
86	SEG85
87	SEG84
88	SEG83
89	SEG82
90	SEG81
91	SEG80
92	SEG79
93	SEG78
94	SEG77
95	SEG76
96	SEG75
97	SEG74
98	SEG73
99	SEG72
100	SEG71
101	SEG70
102	SEG69
103	SEG68
104	SEG67
105	SEG66
106	SEG65
107	SEG64
108	SEG63
109	SEG62
110	SEG61
111	SEG60
112	SEG59
113	SEG58
114	SEG57
115	SEG56
116	SEG55
117	SEG54
118	SEG53
119	SEG52
120	SEG51
121	SEG50
122	SEG49
123	SEG48
124	SEG47
125	SEG46
126	SEG45
127	SEG44
128	SEG43
129	SEG42
130	SEG41
131	SEG40
132	SEG39
133	SEG38
134	SEG37
135	SEG36
136	SEG35
137	SEG34
138	SEG33
139	SEG32
140	SEG31
141	SEG30
142	SEG29
143	SEG28
144	SEG27
145	SEG26
146	SEG25
147	SEG24
148	SEG23
149	SEG22
150	SEG21
151	SEG20
152	SEG19
153	SEG18
154	SEG17
155	SEG16
156	SEG15
157	SEG14
158	SEG13
159	SEG12
160	SEG11

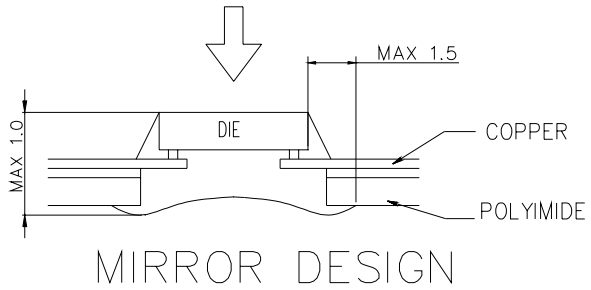
Pin no.	Pin Name
161	SEG10
162	SEG9
163	SEG8
164	SEG7
165	SEG6
166	SEG5
167	SEG4
168	SEG3
169	SEG2
170	SEG1
171	SEG0
172	NC
173	NC
174	NC
175	NC
176	NC
177	NC
178	NC
179	NC
180	NC
181	NC
182	COM0
183	COM2
184	COM4
185	COM6
186	COM8
187	COM10
188	COM12
189	COM14
190	COM16
191	COM18
192	COM20
193	COM22
194	COM24
195	COM26
196	COM28
197	COM30
198	COM32
199	COM34
200	COM36
201	COM38
202	COM40
203	COM42
204	COM44
205	COM46
206	NC
207	NC

SSD0300TR1 TAB details dimensions

Figure 23- SSD0300TR1 detail dimensions

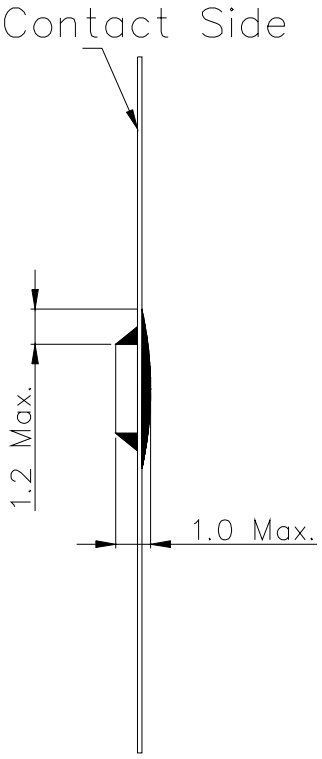


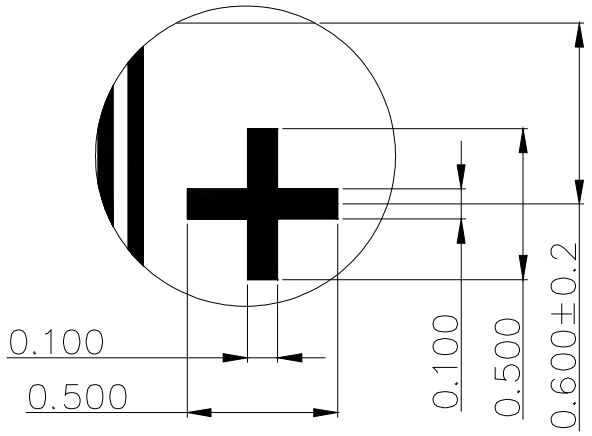




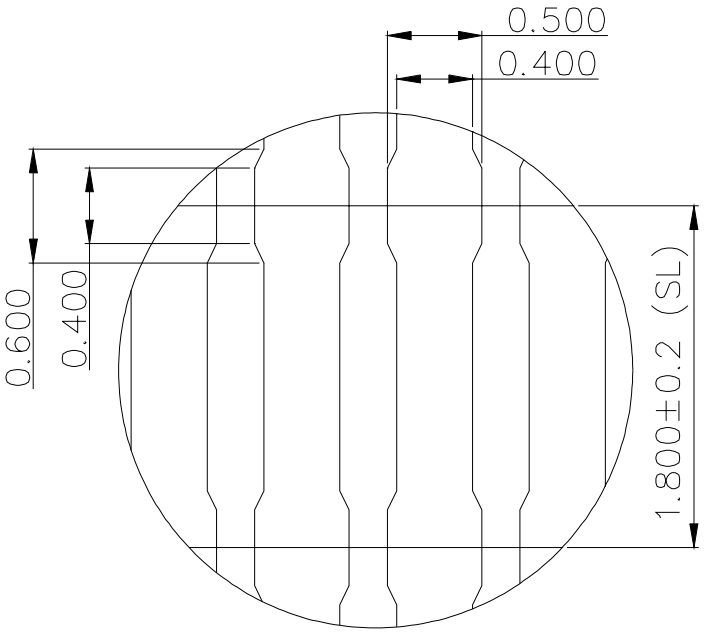
Specification:

1. GENERAL TOLERANCE: ±0.05 mm
2. MATERIAL
   - PI: 75 ± 8 um
   - CU: 18 ± 5 um
   - ADHESIVE: 12 ± 3um
   - SR: 26 ± 14 um
     TOLERANCE ± 0.200 mm
   - FLEX COATING: Min10 um
3. Plating : Sn 0.20 ±0.05 um
4. TAPESITE: 4 SPH,19 mm

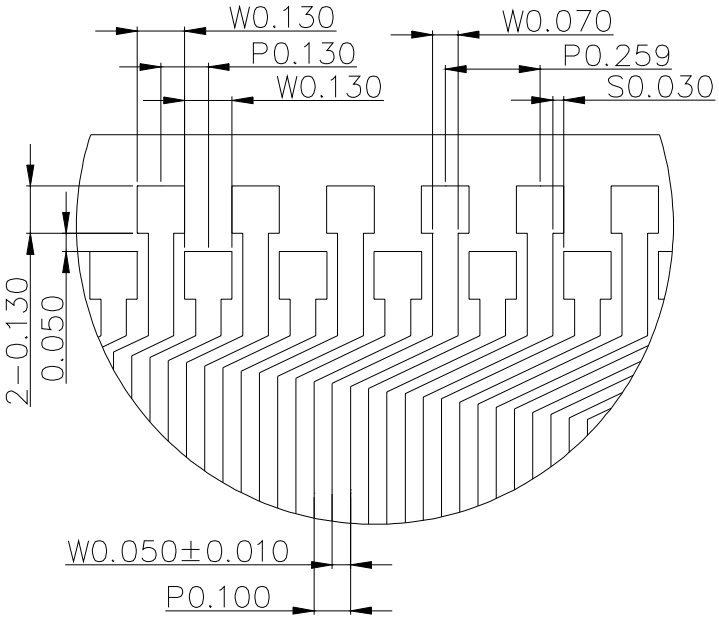




Detail A Scale5:1
Tolerance:0.02mm



Detail B Scale4:1



Detail C Scale5:1

17 SSD0300T3R1 TAB PACKAGE

SSD0300T3R1 pin assignment

Figure 24 - SSD0300T3R1 pin assignment (Copper view)

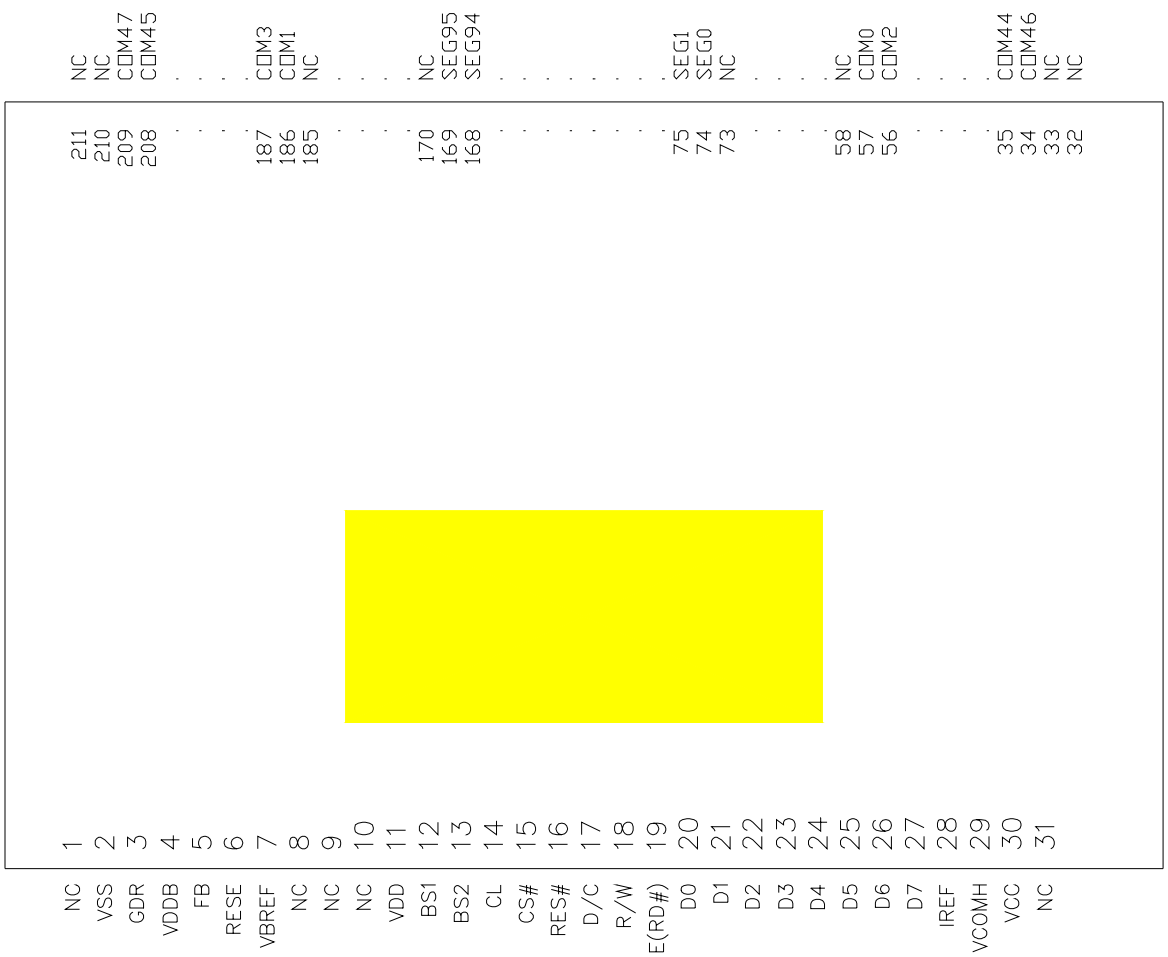


Table 15 - SSD0300T3R1 pin assignment

Pin no.	Pin name
1	NC
2	VSS
3	GDR
4	VDDB
5	FB
6	RESE
7	VBREF
8	NC
9	NC
10	NC
11	VDD1
12	BS1
13	BS2
14	CL
15	CS#
16	RESE
17	D/C
18	R/W
19	E/RD
20	D0
21	D1
22	D2
23	D3
24	D4
25	D5
26	D6
27	D7
28	IREF
29	VCOMH
30	VCC
31	NC
32	NC
33	NC
34	COM46
35	COM44
36	COM42
37	COM40
38	COM38
39	COM36
40	COM34
41	COM32
42	COM30
43	COM28
44	COM26
45	COM24
46	COM22
47	COM20
48	COM18
49	COM16
50	COM14
51	COM12
52	COM10
53	COM8
54	COM6
55	COM4
56	COM2
57	COM0
58	NC
59	NC
60	NC

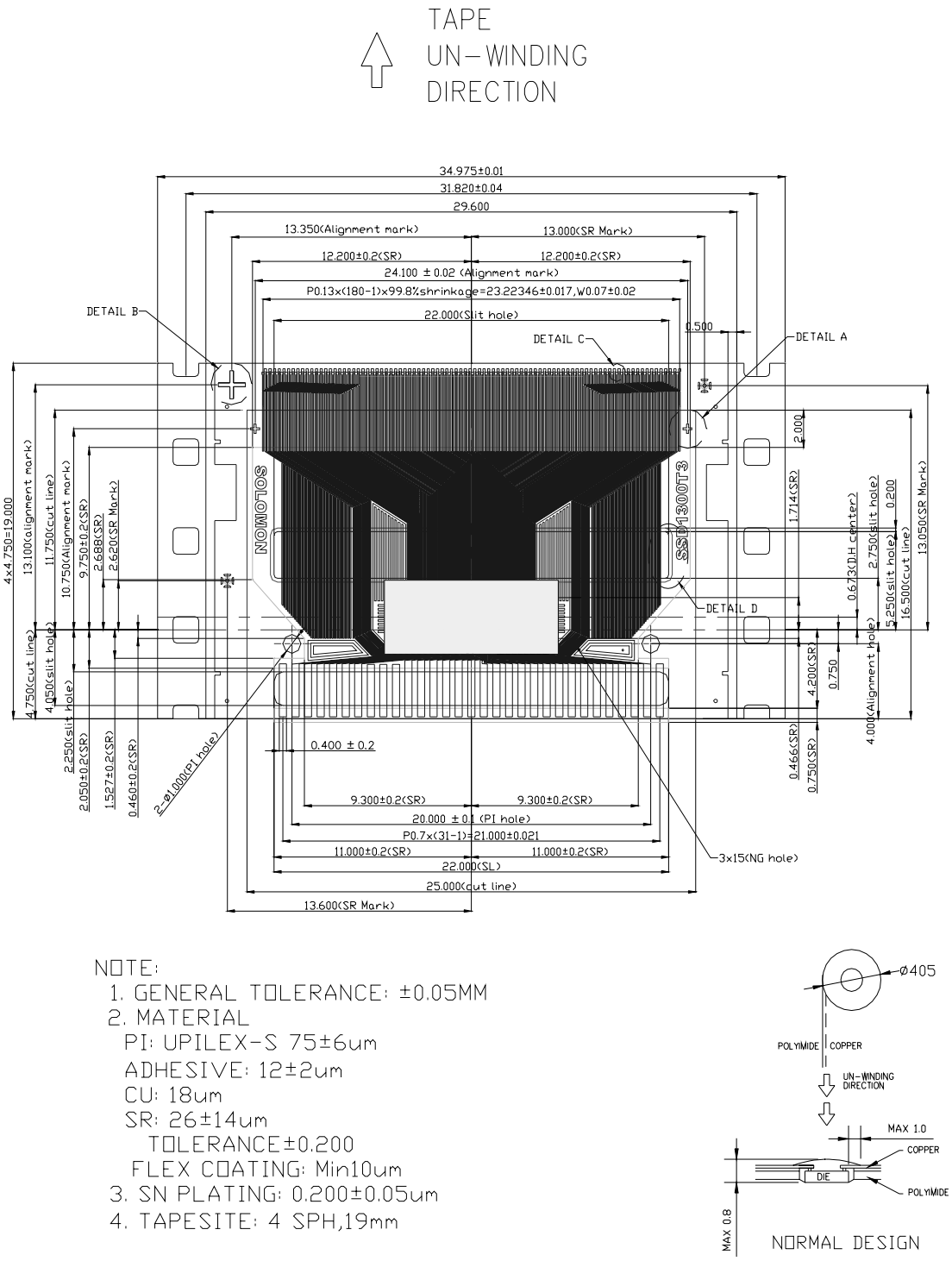
Pin no.	Pin name
61	NC
62	NC
63	NC
64	NC
65	NC
66	NC
67	NC
68	NC
69	NC
70	NC
71	NC
72	NC
73	NC
74	SEG0
75	SEG1
76	SEG2
77	SEG3
78	SEG4
79	SEG5
80	SEG6
81	SEG7
82	SEG8
83	SEG9
84	SEG10
85	SEG11
86	SEG12
87	SEG13
88	SEG14
89	SEG15
90	SEG16
91	SEG17
92	SEG18
93	SEG19
94	SEG20
95	SEG21
96	SEG22
97	SEG23
98	SEG24
99	SEG25
100	SEG26
101	SEG27
102	SEG28
103	SEG29
104	SEG30
105	SEG31
106	SEG32
107	SEG33
108	SEG34
109	SEG35
110	SEG36
111	SEG37
112	SEG38
113	SEG39
114	SEG40
115	SEG41
116	SEG42
117	SEG43
118	SEG44
119	SEG45
120	SEG46

Pin no.	Pin name
121	SEG47
122	SEG48
123	SEG49
124	SEG50
125	SEG51
126	SEG52
127	SEG53
128	SEG54
129	SEG55
130	SEG56
131	SEG57
132	SEG58
133	SEG59
134	SEG60
135	SEG61
136	SEG62
137	SEG63
138	SEG64
139	SEG65
140	SEG66
141	SEG67
142	SEG68
143	SEG69
144	SEG70
145	SEG71
146	SEG72
147	SEG73
148	SEG74
149	SEG75
150	SEG76
151	SEG77
152	SEG78
153	SEG79
154	SEG80
155	SEG81
156	SEG82
157	SEG83
158	SEG84
159	SEG85
160	SEG86
161	SEG87
162	SEG88
163	SEG89
164	SEG90
165	SEG91
166	SEG92
167	SEG93
168	SEG94
169	SEG95
170	NC
171	NC
172	NC
173	NC
174	NC
175	NC
176	NC
177	NC
178	NC
179	NC
180	NC

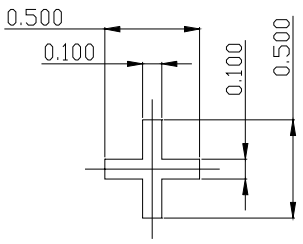
Pin no.	Pin name
181	NC
182	NC
183	NC
184	NC
185	NC
186	COM1
187	COM3
188	COM5
189	COM7
190	COM9
191	COM11
192	COM13
193	COM15
194	COM17
195	COM19
196	COM21
197	COM23
198	COM25
199	COM27
200	COM29
201	COM31
202	COM33
203	COM35
204	COM37
205	COM39
206	COM41
207	COM43
208	COM45
209	COM47
210	NC
211	NC

SSD0300T3R1 TAB details dimensions

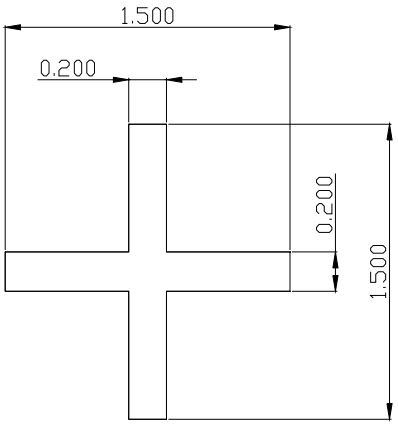
Figure 25- SSD0300T3R1 detail dimensions



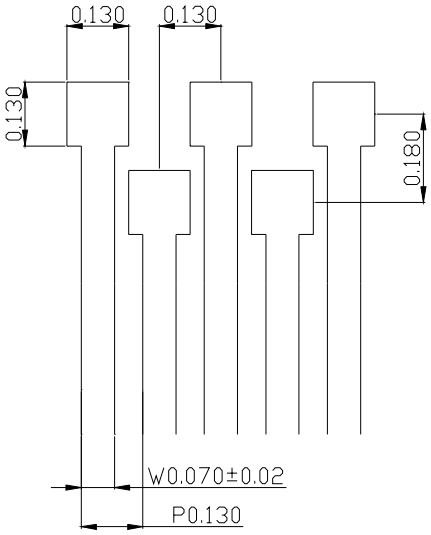
NOTE:
1. GENERAL TOLERANCE: ±0.05MM
2. MATERIAL
   PI: UPILEX-S 75±6um
   ADHESIVE: 12±2um
   CU: 18um
   SR: 26±14um
   TOLERANCE±0.200
   FLEX COATING: Min10um
3. SN PLATING: 0.200±0.05um
4. TAPESITE: 4 SPH,19mm



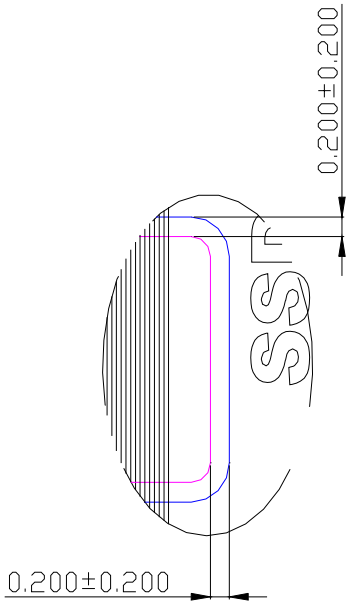
DETAIL A



DETAIL B



DETAIL C



DETAIL D

TAB marking Description

TAB marking is in form of "$2X_6\ X_5\ X_4\ X_3\ X_2\ X_1$", where "2" stands for I^2C TAB and "X"s are the other (normal) marks.

http://www.solomon-systech.com